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IBM Systems Reference Library

IBM 1130 Computing System
Storage Access Channel
Original Equipment Manufacturers' Information

This publication contains information for engineers who plan to attach their equipment to the IBM 1130 Computing System.

Detailed information for the storage access channel is provided, including timing diagrams, line descriptions, and electrical parameters.

The functions of the 1131 and 1133 are also described. The interface points for other IBM devices that normally attach to the 1131 or 1133 are also listed, including voltage and current levels.

A glossary is included in the Appendix.

PREFACE

The interface of original equipment manufacturers' input/output devices to the IBM 1131 Central Processing Unit (CPU) requires an intimate knowledge of the internal operation of the CPU.

The purpose of this publication is to provide detailed descriptions of the timing and internal operations of the CPU and to provide necessary data on the physical and electrical parameters of the storage access channel interface.

The IBM 1133 Multiplex Control Enclosure, if attached to the 1131 CPU, interfaces to the storage access channel, and in turn, provides the storage access channel II for the original equipment manufacturer (OEM) that wishes to use the features of both the 1131 and the 1133.

The electrical design considerations begin with the choice of a circuit family in the 30-nanosecond range that is suited for the operating voltages and currents defined in this publication.

Original equipment manufacturers are cautioned that specifications are subject to change by IBM. The data contained herein is current as of December 1968. Complete wiring diagrams at the latest engineering level are included in each machine shipment.

Sixth Edition (December 1968)

This publication (Form A26-3645-5) is a major revision, replacing and making obsolete A26-3645-4. The section entitled "Storage Access Channel Line Descriptions" has extensive modification. Other changes to the text are indicated by a vertical bar to the left of the text; changes to figures are indicated by the symbol (•) to the left of the figure title.

Significant changes or additions to the specifications contained in this publication are continually being made. When using this publication in connection with the operation of IBM equipment, check the latest SRL Newsletter for revisions or contact the local IBM branch office.

The illustrations in this manual have a code number in the lower corner. This is a publishing control number and is not related to the subject matter.

Copies of this and other IBM publications can be obtained through IBM Branch Offices.

This manual was prepared by the IBM Systems Development Division, Product Publications, Department G24, San Jose, California 95114. Send comments concerning the contents of this manual to this address.

CONTENTS

The IBM 1130 Computing System consists of two logical functions: the input and output of data in a variety of forms, and the controls necessary to efficiently manipulate this data.

The IBM 1131 Central Processing Unit functions as a nerve center – requesting and accepting input data, performing the calculations required, and producing the resultant data – all under stored program control.

Input/output (I/O) devices transfer information to or from the 1131 CPU. Paper tape, punched cards, mark-sense documents, magnetic disk storage, and communication transmission are provided as input from IBM devices. Data output from the CPU may be in the form of printed documents, graphic displays, punched cards, punched paper tape, communication transmission, and magnetic disk storage.

The storage access channel (SAC) provides a convenient means for the OEM user to gain access to the 1131 CPU input and output lines to attach OEM input/output devices.

The OEM user interfacing to the 1131, either through the SAC or another interface in the CPU, should become throughly familiar with I/O operation, certain critical timings, and the philosophy of 1130 interrupt and cycle-steal operations. Operations requiring multiple cycle-steals deserve special timing considerations to avoid compromising the performance of the system.

The descriptions presented in this manual are a summary of the operation of the 1131 CPU, the function of the 1133, and the detailed descriptions of the storage access channel (SAC I and SAC II).

Related Publications

Detailed theory of operation, physical planning information, and general engineering information for the IBM 1131 Central Processing Unit can be obtained from the following IBM publications.

IBM 1130 Bibliography (Form A26-5916): The bibliography lists applicable publications and related materials in subject code and machine-type number sequence and provides a brief abstract of each publication.

By reviewing these indexes and abstracts, you may select those items of interest to your installation and keep abreast of other materials which may be useful at some future time.

IBM 1130 Functional Characteristics (Form A26-5881): This reference manual contains basic programming and operating information for the 1130 Computing System. It explains the functional aspects of the system in detail, and describes the operational characteristics in terms of program instructions, input/output operations, and central processing unit console displays and functions. Since this is a reference manual, the material presented assumes some prior knowledge of stored program computers.

IBM 1130 Operating Procedures, (Form A26-5717): This publication is a guide to the operation of the 1130 system. It describes the control keys, indicator lights, and principles of operation of all input/output devices that attach to the 1130 system.

IBM 1130 Installation Manual – Physical Planning (Form A26-5914): This publication contains physical planning information for the installation of an 1130 system. It includes dimensions, weights, cable locations and available lengths, service clearances, and other necessary physical information for each unit of the system. Environmental and electrical requirements are also included. Photographs and drawings are used throughout the text, and a summary table of physical planning specifications is provided.

Requests for publications, engineering information, or engineering documents should be forwarded to an IBM sales office.

The IBM 1131 Central Processing Unit (CPU) is a compact, versatile component of the IBM 1130 Computing System. The design is oriented to the operator, and a minimum of training and experience with computing systems is sufficient for engineering and research personnel to utilize the 1131 to solve problems.

The console displays the data in the various registers, counters, and other areas of the CPU. Console switches provide for the control of the operation and for the entry of data from the console keyboard. The console printer provides printed output of the data in core storage.

Three models of the 1131 CPU are available: model 1, model 2, and model 3.

The model 1 and model 2 each have a 3.6 microsecond core storage cycle time. Core storage cycle time is the time required to enter a word into or retrieve a word from core storage. Model 2 has a single disk storage.

The model 3 has a 2.2 microsecond core storage cycle and also has a single disk storage.

Single disk storage is an auxiliary storage device housed within the 1131 CPU enclosure. It consists of a single disk drive and a removable disk cartridge. Storage capacity of each cartridge is 512,000 sixteen-bit words. The data transfer rate of the disk storage is 720,000 bits per second. The removable disk cartridge provides easy access to data or to entire programs. Additional disk cartridges can be stored off-line and put on-line as needed, thus providing virtually unlimited off-line storage capacity.

Core Storage

The 1131 main storage in the CPU uses magnetic cores for data and program instruction storage. Core storage capacity is 4,096 (4k) to 32,768 (32k) 16-bit words, depending upon the model used:

	A	B	C	D
Model 1	4k	8k	—	—
Model 2	4k	8k	16k	32k
Model 3	—	8k	16k	32k

A 16-bit word can be placed into core storage or retrieved from core storage in one storage cycle; 3.6 microseconds for models 1 and 2 and 2.2 microseconds for model 3.

Addressing

Each word in core storage has an individual address. Addresses range from 0 to 32767. The high-order address is contiguous with the low-order address, a fact that provides for "wraparound addressing". In sequential processing of addresses, the address 4095, 8191, 16383, or 32767 (depending upon capacity installed) is followed by address zero without further specification by the CPU. Certain addresses in core storage are commonly used by the CPU for special purposes.

Reserved Core Storage Locations

The following core storage decimal addresses are reserved for the specific use of the CPU:

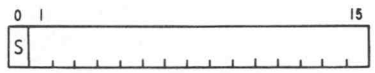
Core Storage Address	Description
00001	Index Register 1
00002	Index Register 2
00003	Index Register 3
00008-00013	Interrupt Vectors
00032-00039	1132 Printer Scan Field

DATA FORMAT

Data in the 1131 CPU core storage is in fixed-point binary form. Each number is treated as a signed integer; positive numbers are in true binary with a sign of 0, and negative numbers must be stored and operated upon in 2's complement form with a sign bit of 1. Complementing is done by inverting each bit of the number (including the sign bit) and adding 1 to the low-order bit. The following example illustrates this.

Positive number	0001101001001100
Inverted	1110010110110011
Add 1	1
Resulting negative number	1110010110110100

Data is stored as either a single precision word or a double precision word. A single precision data word comprises 16 bits; bit positions are numbered 0 to 15 from left to right. The high-order bit (0) is the sign position.



Single Precision Data Word Format

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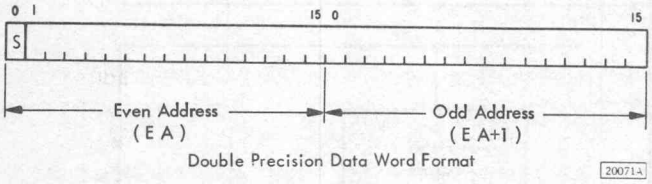
The largest base-10 (decimal) values of single precision words are +32,767 and -32,768. A double precision data word contains 32 bits, and is composed of two sequential single precision words. The high-order bit (0) is the sign position.



Double Precision Data Word Format

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A double precision data word is addressed by the leftmost word, which has an effective address (EA) that must be even.

The highest base-10 values of double precision data words are +2,147,483,647 and -2,147,483,648.

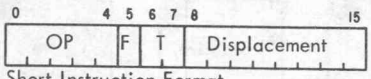
The largest positive number ($2^{31}-1$) is one less than the largest negative number (2^{31}) because the sign (0 for plus, 1 for minus) is, arithmetically, part of the number.

All CPU storage is in binary form, and internal addressing and console displays are in 16-bit binary notation. Because of the ease of operation with 16-bit words in the hexadecimal number system (base 16), all programming systems for the IBM 1130 Computing System use this notation.

INSTRUCTION FORMATS

Program instructions in the 1130 system are in either short or long format.

Short Instruction Format



Short Instruction Format

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OP (Operation) Code: These five bits specify the operation performed.

F (Format): The F bit controls the instruction format. A zero (0) indicates a short instruction format; a one (1) designates a long instruction format.

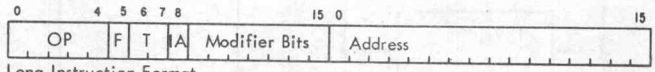
T (Tag): These two bits specify the instruction counter or the specific index register (XR) that contains the data to be used with this instruction for EA generation.

Displacement: This field may be used as a shift modifier for shift instructions or as a displacement in other instructions.

When used as a displacement, the data in these eight bits is added to the data in the register specified by the tag bits. The result is the effective address (EA). If the displacement amount is negative, it is in 2's complement form, and the sign is in bit position 8.

When used as a shift modifier, this field specifies the number of positions the accumulator is to be shifted.

Long Instruction Format



Long Instruction Format

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The first eight bit positions of the long instruction are the same as the short format. The remaining bit positions of this double precision word are used as follows.

IA (Indirect Address): A zero indicates a direct address (contained in the second word). A 1-bit in this position designates an indirect address. Bit positions 9 through 15 have various uses as modifiers.

Address: These 16 bits contain the address which may be used in its current form or modified by indirect addressing and/or EA modification.

REGISTERS

The CPU has auxiliary storage areas, called registers, that are used to store data during the performance of operations directed by the stored program. Each register has a distinct purpose and is concerned with a specific type of data. Closely interrelated, they provide the CPU with the necessary functions to provide the results required. (See Figure 1.)

Index Registers

Index registers are located in core storage and are used to contain data added to an instruction to provide an effective address. In a short instruction the amount in the displacement field of the instruction is added to the amount in the index register specified by the tag bits (6 and 7). The result becomes the effective address used by the instruction in the operation specified by the OP code.

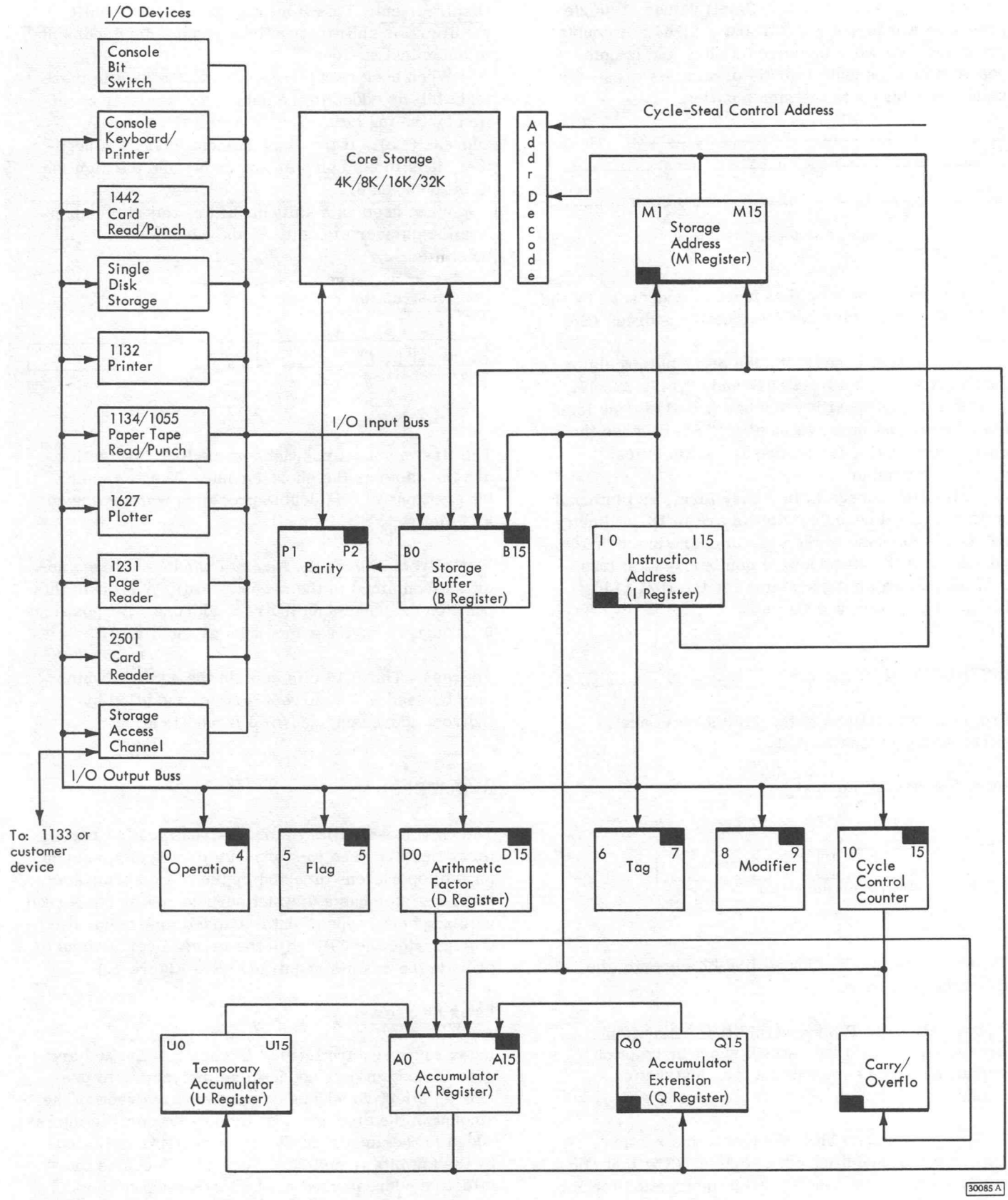


Figure 1. CPU Controls and Data Flow

Register Number	Instruction Code Bits 6 and 7	Core Storage Location
1	01	00001
2	10	00002
3	11	00003

Machine Registers

The ten registers in the CPU are basic to the system and are functional elements of the CPU. Each register operates as necessary to enable the CPU to provide the results specified by the program. The abbreviation for each register name is the designation by which it is usually identified.

ACC (Accumulator): This 16-bit register contains the result of an arithmetic operation. It can be loaded from or stored in core storage, shifted right or left, and otherwise manipulated by specific arithmetic and logical instructions.

EXT (Accumulator Extension): This 16-bit register is the low-order extension of the ACC. It is used during multiply and divide operations, shifting of the ACC and EXT, and double-word arithmetic.

TAR (Temporary Accumulator): This 16-bit register is the image of the ACC and is used to store the contents of the ACC during effective address computation.

AFR (Arithmetic Factor Register): This 16-bit register holds one operand during arithmetic and logical operations. (The other operand is provided by the ACC.)

SBR (Storage Buffer Register): This 16-bit register is the buffer between the CPU and core storage, and every word of data transferred into or out of core storage passes through the SBR.

SAR (Storage Address Register): This 15-bit register contains the address pertaining to each reference to a core storage word.

IAR (Instruction Address Register): This 15-bit register holds the address of the next sequential instruction.

OP (Operation Register): This 5-bit register holds the OP code of the instruction being performed.

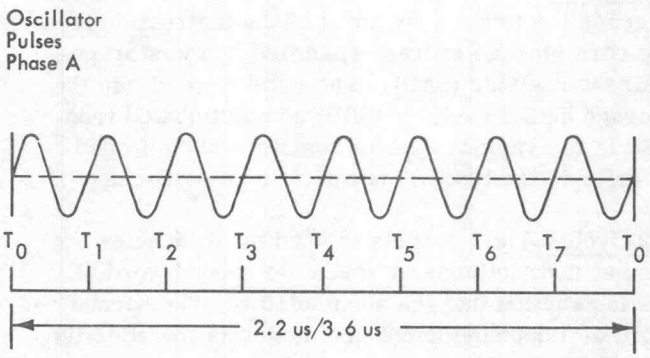
TAG (Operation Tag Register): This 3-bit register contains the F and T bits of the instruction. It controls the instruction length and selects the index register.

CCC (Cycle Control Counter): This 6-bit register is used primarily to count CPU cycles and control shift operations.

MACHINE CYCLES

There are two basic types of machine cycles used by the 1131 to perform all operations: the instruction (I) cycle and the execution (E) cycle. In the model 1 and model 2, each machine cycle requires 3.6 usec and consists of 8 pulses of the 2.25 MHz clock oscillator, which generates the basic timing for the CPU. In the model 3, each machine cycle requires 2.2 usec and consists of 8 pulses of the 3.64 MHz clock oscillator, which generates the basic timing for the model 3 CPU.

The phase A pulses generated by the clock oscillator are accurate within .05 percent.



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Instruction Type	I Cycle Required			
	I - 1	I - 2	I - X	I - A
Single Word	X			
Single Word With Indexing	X		X	
Double Word	X	X		
Double Word With Indexing	X	X	X	
Double Word With Indirect Addressing	X	X		X
Double Word With Indexing and Indirect Addressing	X	X	X	X

11553

Instruction Cycles (I-Cycles)

The 1130 instruction set consists of 29 discrete instructions. The instruction cycle is used to interpret the type of operation to be performed, the data locations, and the machines involved. Single (one

16-bit word) or double (two 16-bit words) format instructions can be used to give the CPU added flexibility. Instructions fall into five general categories: load and store, arithmetic and logic, shift, branch, and input/output. In this publication, descriptions are mainly concerned with the input/output type of instruction.

Each I-cycle requires one basic machine cycle. There are up to four I-cycles:

I-1
I-2
I-X
I-A

The number of I-cycles used is dependent upon the type of operation and the addressing method specified by the program. (See Figure 2.)

I-1 Cycle: The I-1 cycle is used by all instructions. It reads the first 16-bit word of the instruction from the core storage address specified by the storage address register (SAR). The word is read into the storage buffer register (SBR) and distributed from SBR to the various control registers and decoded to indicate the type of operation to be performed.

I-2 Cycle: The I-2 cycle is used by all double-format instructions. It reads the second word of the instruction into the accumulator. The second word of a double-format instruction is the effective address unless it is to be modified by indexing or indirect addressing.

I-X Cycle: The I-X cycle is used only by instructions that specify indexing or indirect addressing. The contents of the index register specified by the tag bits (bits 6 and 7) of the instruction are read and added to the contents of the accumulator.

The contents of the accumulator is always considered a positive (absolute) value. The instruction, as it appears in core storage, is not changed by the indexing operation.

When an address is indexed and indirect, the indexing procedure takes precedence. The resultant effective address after indexing is the new indirect address. One indexing and one indirect addressing operation can be done for each instruction.

I-A Cycle: The I-A cycle is used only for indirect addressing. It reads a direct address from the core storage location specified by the indirect address in the accumulator, and transfers the direct address to the accumulator to replace the indirect address.

A direct address is the address of data in core storage; an indirect address is the address in which a direct address is stored. For most 1130 instructions, the address generated during the I-1, I-2, and I-X cycles is a direct address.

Execution Cycles (E-Cycles)

Execution cycles (Figure 3) are used to perform the operation specified in the associated instruction cycle. Each E-cycle requires one machine cycle. The number of machine cycles required depends upon the specific operation to be performed. The following operations are complete at the end of I-cycles and require no E-cycles:

1. Wait (00000).
2. Shift Left (00010) (if not a Shift Left and Count).
3. Shift Right (00011).
4. Load Status (00100).
5. Branch and Store I Register (01001) (if condition is not met).
6. Branch or Skip on Condition (01001).
7. Load Index (01100) (if no index register is specified).
8. MDX (01110) (if flag =0 and tag =00).

When the execution time for an operation is complete, the CPU proceeds to the next sequential instruction.

There may be up to three E-cycles taken to complete the execution phase of the operation.

E-1
E-2
E-3 (used for XIO only)

E-1 Cycle: This cycle transfers the effective address (EA) to the SAR and reads the IOCC control word (EA+1) into the SBR. This word contains the area, function, and modifier bits. (See input/output control command.)

E-2 Cycle: This cycle reads the address word portion of the IOCC (EA) to the SBR, and also routes it through the ACC to the SAR for use in the E-3 cycle of an XIO Read or Write instruction.

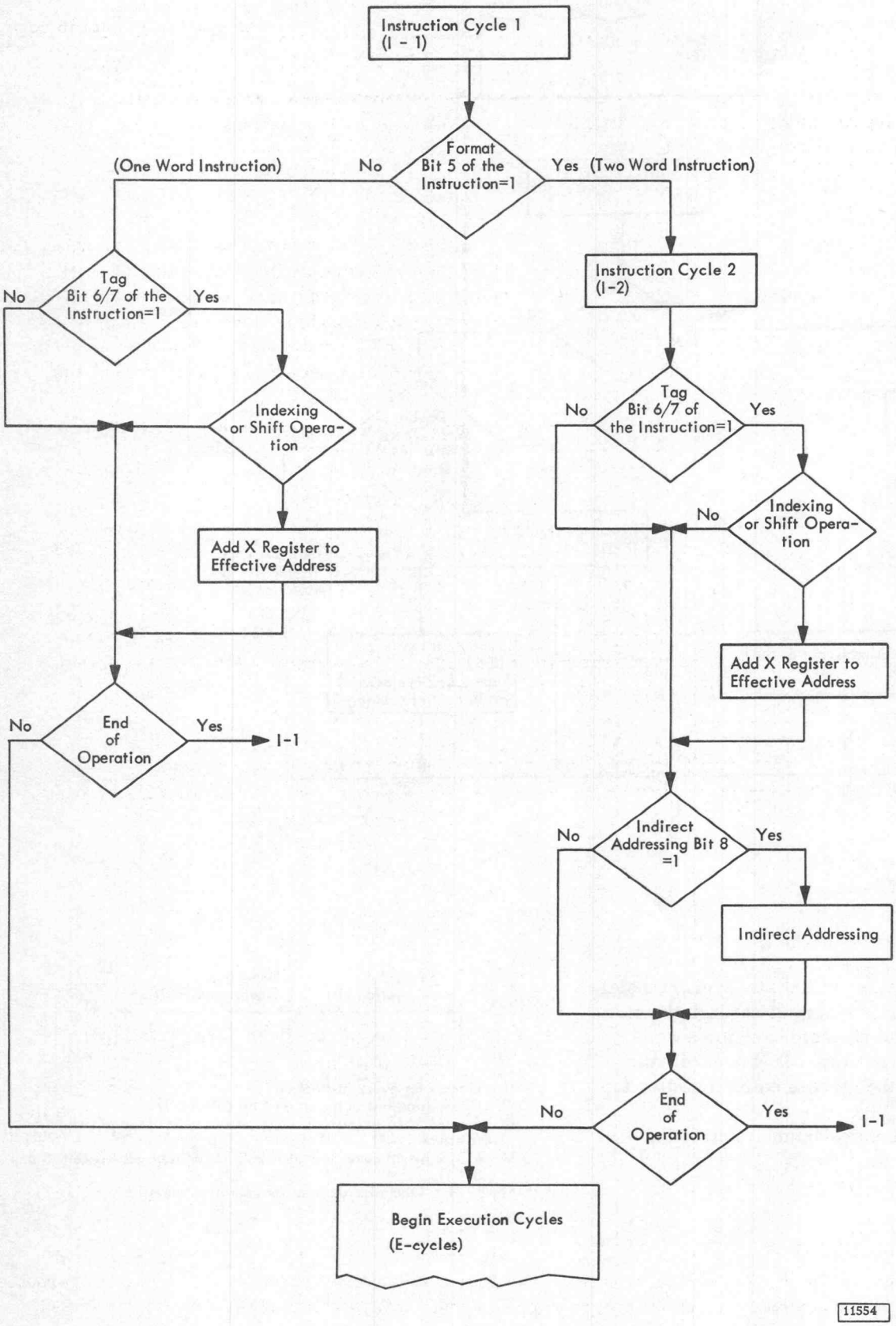


Figure 2. Instruction Cycles

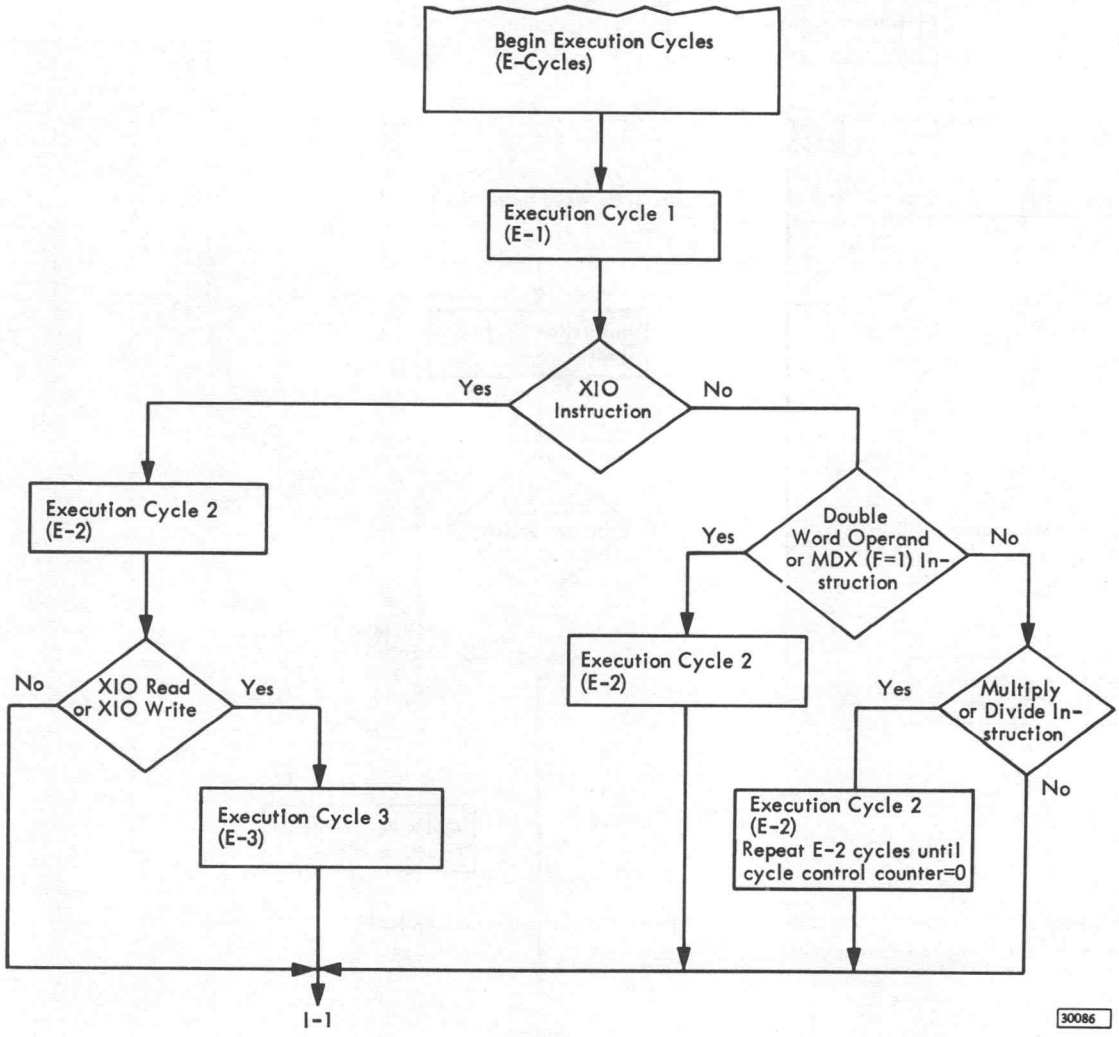
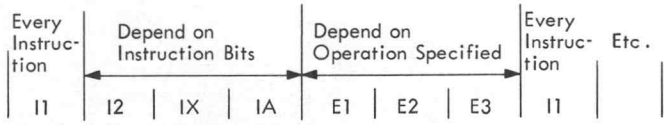


Figure 3. Execution Cycles

E-3 Cycle: For a read operation this cycle transfers a 16-bit word from the I/O adapter through the storage buffer register into core storage; for a write operation this cycle transfers a 16-bit word from core storage through the storage buffer register to the I/O adapter.

The machine cycles are summarized in the following chart.



I1 Occurs for every instruction.
I2 Depends on instruction format bit (bit 5 = 1).
IX Occurs when index register is used to compute effective address (bit 6 or 7 = 1).
IA Occurs when computed address is an indirect address (bits 5 and 8 = 1).
E1, E2, E3 Occur as required for operation specified.

13198

Two methods are used to control I/O devices and to effect the transfer of data between core storage and attached I/O devices.

1. Direct program control (interrupt mode): initiated by XIO instructions. Each 16-bit word transfer or physical action of an I/O device is initiated by an individual XIO instruction.
2. Combined control (cycle-steal mode): initiated by XIO instructions. Data transfers or physical action of an I/O device are controlled by a combination of cycle-steal operations and XIO instructions.

The basic differences between the two methods are shown in the following chart:

Cycle	Direct Program Control	Combined Control
E-1 Cycle	Transfer Control Word to I/O Adapter	Same
E-2 Cycle	Data Address to SAR if Read or Write. Data table address for Initiate Read or Write. Control data. Input data for Sense.	Data Address to Cycle Steal Address Register. Terminate Op.
E-3 Cycle	Transfer data word to or from I/O Adapter using SAR address. Terminate Op. Can also request data or accept data by issuing a write or read command.	Asynchronously interrupts to I/O subroutine to inform CPU that the previous command has been completed.
Cycle Steal Cycle	None	Transfer data word to or from I/O Adapter using Cycle Steal Address. Take C.S. cycles when needed for subsequent data word transfers.

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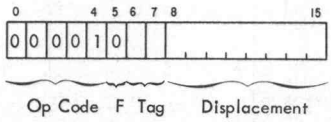
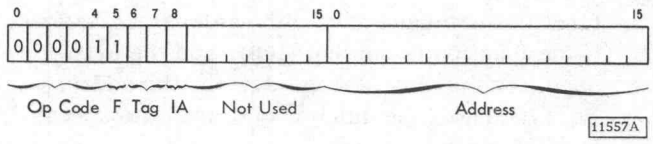
XIO Instruction

The XIO instruction specifies the function to be performed by an I/O device and specifies the core storage location of a two-word input/output control command (IOCC) which further defines the operation. The XIO instruction can have either a one-word or a two-word format.





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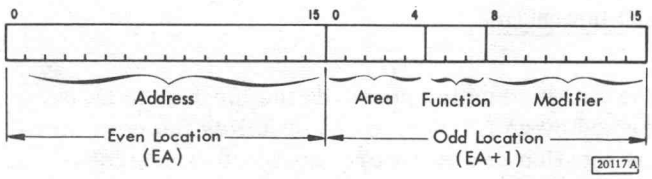
Input/Output Control Command

The core storage location of the appropriate I/O control command (IOCC) for the operation is specified in the address portion of the XIO instruction. The address of the IOCC must be even. Seven IOCC functions are provided for the 1130:

Read
Write
Initiate read
Initiate write
Control
Sense device
Sense interrupt

All I/O control commands have four parts: the address, area, function, and modifier, as shown below.



Address

The meaning of this 16-bit field is determined by the setting of the function field in the I/O control command:

1. If the function is initiate write (101) or initiate read (110), the address field specifies the starting address (low order) of a table in storage. The table contains data and control information. Initiate write and initiate read functions are used only with cycle-steal devices.
2. If the function is control (100), and the area specifies the disk storage device, the address field indicates the number of tracks the access mechanism is to move.
3. If the function is sense device (111) or sense interrupt (011), the address field is ignored. In this case the selected I/O device or interrupt level places its status code into the accumulator.
4. If the function is write (001) or read (010), the address field specifies the core storage location of the data word.

Area

This five-bit field identifies the I/O device. The 1130 area codes for IBM devices are:

Area Code		
Decimal	Binary	Device
0	00000	Not available
1	00001	Console Keyboard & Printer
2	00010	1442 Card Read Punch
3	00011	1134 Paper Tape Reader & 1055 Paper Tape Punch
4	00100	Internal Single Disk Storage
5	00101	1627 Plotter
6	00110	1132 Printer
7	00111	Console Entry Switches
8	01000	1231 Optical Mark Page Reader
9	01001	2501 Card Reader
10	01010	Synchronous Communications Adapter
17	10001	2310 Disk Storage Drive 1
18	10010	2310 Disk Storage Drive 2
19	10011	2310 Disk Storage Drive 3
20	10100	2310 Disk Storage Drive 4
21	10101	1403 Printer

Note: Area Codes 22-31 are reserved for IBM RPQ* activity. However, the user may use any area code not presently used by his system.

Function

The seven I/O control command functions are specified by the three-bit function code. The function codes and the associated I/O functions are:

000 - Not available

001 - Write. This code is used to transfer a 16-bit word from core storage to an I/O device. The core storage location is specified by the address field of the I/O control command.

010 - Read. This code is used to transfer a 16-bit word from a selected I/O device to core storage. The core storage location is specified by the address field of the I/O control command.

011 - Sense interrupt. This code is used to determine which one of a group of devices on an interrupt level is requesting service. The status of the requesting device is loaded into the accumulator.

100 - Control. This code causes the selected I/O device to interpret the address or modifier field as a specific control action, such as forms spacing or stacker selection.

101 - Initiate write. This code initiates a write operation on cycle-stealing devices. Subsequent transfer of data from core storage is controlled by the device.

110 - Initiate read. This code initiates a read operation on cycle-stealing devices. Subsequent transfer of data from the device to core storage is controlled by the device.

111 - Sense device. This code loads the ACC with the device status word (DSW) for the device specified in the IOCC. The status indicators are reset by specifying modifier bits as follows: bit 15 for the highest level to which the device is connected, bit 14 for the next highest level, and so on.

*Request Price Quotation from IBM for custom-designed attachments.

Modifier

The eight-bit modifier field provides additional definition for the function field or the area field.

Input/Output Interrupt Operation

Input/output interrupts are caused by a request for service from an I/O device or by the termination of an I/O operation. The interrupt facility provides an automatic branch from the normal program sequence in order to react to an external request or condition.

At the completion of any program instruction, any pending interrupt requests are serviced if no higher level interrupt is in progress.

Input/output interrupts are assigned priority levels to allow the most efficient use of all attached I/O devices in the system.

Level	Device
0	1442 Card Read Punch (column read, punch)
1	1132 Printer, synchronous communications adapter
2	Disk storage, storage access channel (SAC)
3	1627 Plotter, SAC
4	1442 (operation complete); Keyboard/Console Printer; 1134 Paper Tape Reader; 1055 Paper Tape Punch, 2501 Card Reader, 1403 Printer, 1231 Optical Mark Page Reader, SAC
5	Console (program stop switch, and interrupt run), SAC

Conditions causing I/O interrupt requests are preserved in the device status word (DSW) of the I/O devices until the interrupt is accepted by the CPU.

The sequence of events after an interrupt request is received is:

1. Instruction in progress is allowed to continue to completion.
2. Interrupt request is accepted if a higher level interrupt is not in progress.
3. Branch to an appropriate interrupt subroutine to service the request.
4. Housekeeping program routines must store all registers and linkage addresses to allow mainline program to continue after the interrupt is serviced.
5. Examine the interrupt level status word (ILSW) to determine the interrupting device.
6. Examine the device status word of the interrupting I/O device to determine the action required to service the request.
7. Service the request and restore the necessary register and address information to resume the mainline program operation or to service other interrupts.

Device Status Word (DSW)

The DSW contains one bit of information for each indicator within the device. These usually fall into three categories: (1) error or exception interrupt conditions, (2) normal data or service-required interrupts, and (3) routine status conditions.

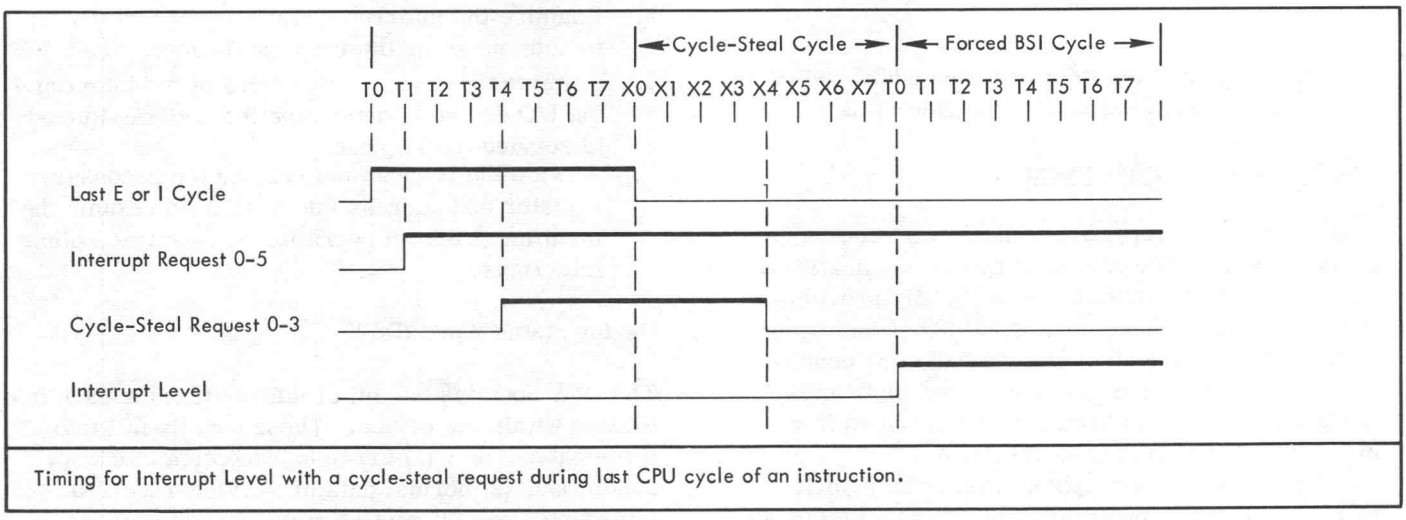
Cycle-Steal Operation

A cycle-steal request may be honored at the end of any core storage cycle. Cycle stealing allows an external device to intervene during the processing of a CPU operation and use one or more core storage cycles in order to communicate directly with CPU core storage. At the completion of the cycle-steal operation, CPU operation is resumed at the point where the cycle-steal request occurred.

Figure 4 illustrates a cycle-steal request preempting the CPU operation while a cycle-steal cycle is taken.

Cycle-Steal Clock

A separate clock, the cycle-steal clock, provides timing pulses during the cycle-steal operation. When a cycle-steal request is issued by the external device, the request is honored at the end of the present machine cycle if a higher priority level is not being serviced. The priority trigger is set, causing the CPU core storage addressing to be blocked; the external device generates a core storage address which is gated to the core storage addressing circuits; the CPU clock is prevented from advancing; and the cycle-steal clock is allowed to run. Both the CPU clock and the cycle-steal clock are generated from a 2.25 or 3.64 megahertz crystal-controlled oscillator in the 1131 CPU.



● Figure 4. Cycle-Steal Request Illustration

The IBM 1133 Multiplex Control Enclosure was developed to expand the I/O capabilities of the basic 1130 system.

The channel multiplexer is an integral part of the 1133 and provides certain controls and timings for the IBM devices attached to the 1133.

Since the 1133 attaches to the SAC in the CPU, the SAC lines are repowered in the 1133 to provide the storage access channel II. In every case, the line descriptions for the SAC also apply to SAC II. However, because of additional cable length and delay of the electronic circuits in the channel multiplexer, certain critical timings must be considered. These considerations are included in the "Storage Access Channel Line Descriptions." Also, the cycle-steal level 1 line becomes the channel multiplex cycle-steal level 6 at the SAC II interface.

The 1133 contains power supplies and power sequencing circuits and, in addition to the channel multiplexer, can accommodate four 2310 Model B disk storage adapters, a 1403 Printer adapter, and a storage access channel II adapter. Power for future expansion within the 1133 is also provided.

Channel Multiplexer

The functions of the channel multiplexer are as follows:

Provides a communication path between external I/O devices or systems and the 1131 processor.

Provides attachment points for IBM 2310 Model B Disk Storage drives, an IBM 1403 Printer, and/or the storage access channel II.

The channel multiplexer circuits provide signal powering, timing levels, E-cycle levels, core storage addressing facilities, and a cycle-steal request priority scheme for the IBM devices attached to it. (See Figure 5.) The cycle-steal priority is also provided to SAC II, which is on multiplex level 6.

Cycle-Steal Priority Levels

Data transfers to or from core storage and the I/O devices attached to the SAC may be in either the cycle-steal or the interrupt mode. The SAC attachment, including the channel multiplexer, is on CPU cycle-steal level 1. This level is subdivided by the channel multiplexer into 12 levels: multiplexer cycle-steal levels 0-11. The cycle-steal priority levels for the 1130 system with SAC, 1133, and SAC II are as follows (the lower the level, the higher the priority):

CPU cycle-steal level 0 – Single Disk Storage (in the CPU)
CPU cycle-steal level 1 – SAC (see the multiplex levels below)
CPU cycle-steal level 2 – 1132 Printer
CPU cycle-steal level 3 – 2501 Card Reader

Cycle-steal level 1 is subdivided by the channel multiplexer (when the 1133 is attached to SAC) as follows:

Multiplex level 0 – 1st 2310 Disk Storage Drive
Multiplex level 1 – 2nd 2310 Disk Storage Drive
Multiplex level 2 – 3rd 2310 Disk Storage Drive
Multiplex level 3 – 4th 2310 Disk Storage Drive
Multiplex level 4 – Reserved (RPQ)
Multiplex level 5 – Reserved (RPQ)
Multiplex level 6 – SAC II (user's OEM device)
Multiplex level 7 – 1403 Printer
Multiplex level 8 – Reserved
Multiplex level 9 – Reserved
Multiplex level 10 – Reserved
Multiplex level 11 – Reserved (RPQ)

The above assignments are given for consideration of expansion for the user that may wish to expand his system at a later date. The cycle-steal levels listed as "Reserved (RPQ) " are for IBM RPQ* activity.

Interrupt Priority Levels

The interrupt levels assigned by the OEM user may be levels 2, 3, 4, or 5. (The lower the level, the higher the priority.) Levels 0 and 1 are reserved

*Request Price Quotation from IBM for custom-designed attachments.

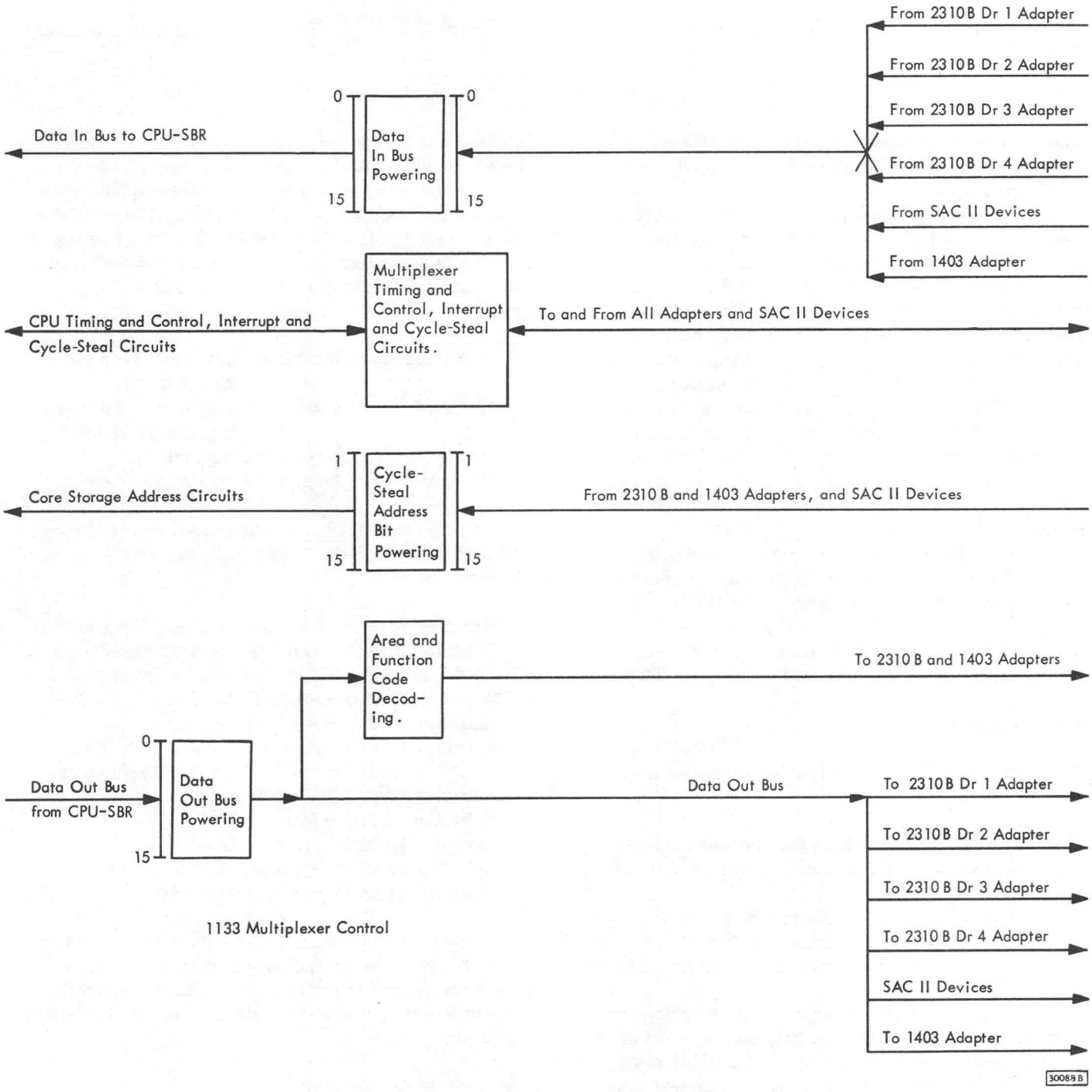
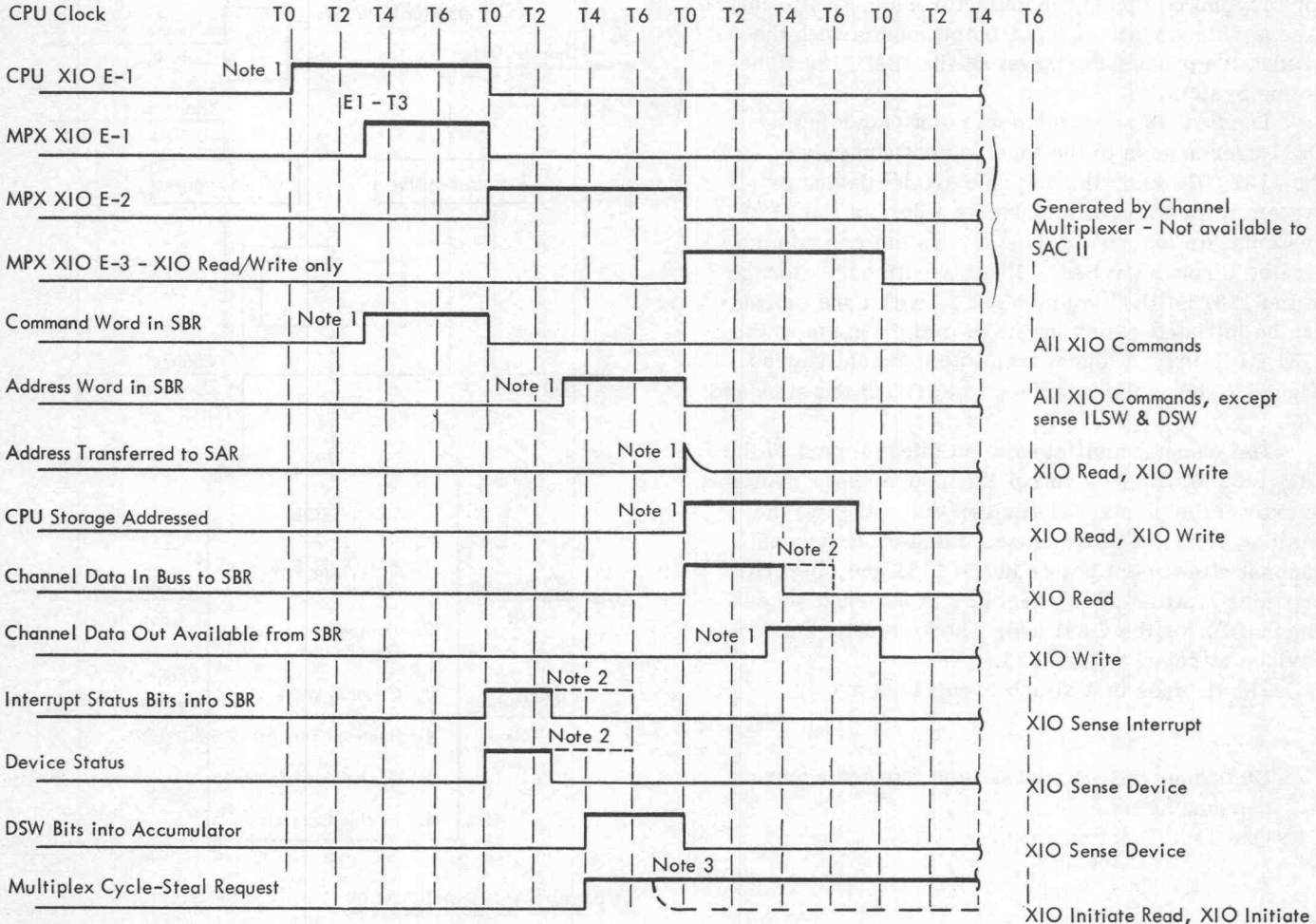


Figure 5. 1133 Controls and Data Flow

for the IBM 1442 Card Read Punch (level 0), and the IBM 1132 Printer and the Synchronous Communications Adapter (level 1). If the 1442 is not used in a system configuration, level 0 is unassigned, and the highest priority is level 1.

Channel Multiplexer Timing

The channel multiplexer timing diagram is shown in Figure 6.



Notes:

1. Generated by the CPU.
2. Dash line represents the additional allowable time the signal may remain up without affecting the operation.
3. This signal not allowed to drop during the following time interval: Trailing edge of T4/X4 to the trailing edge of T7/X7.

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● Figure 6. Channel Multiplexer Timings

The storage access channel (SAC) provides a means for original equipment manufacturers (OEM) to interface a wide variety of input/output media with the productive processing power of the IBM 1130 Computing System.

The SAC is an attachment point providing the OEM user access to the input/output controls of the 1131 CPU and allowing an external device or system to function efficiently as a part of the 1130 system. An external device or system can communicate, through the SAC, directly with core storage in the 1131 CPU. Communication with core storage can be initiated either by the stored program in the 1131 CPU or by a signal from the external source. Figure 7 shows the interface to SAC and the standard I/O.

The channel multiplexer (an integral part of the IBM 1133 Multiplex Control Enclosure) was developed to expand the number of devices that attach to the basic system. The 1133 uses the storage access channel attachment points in the 1131 and, in turn, provides similar attachment points (storage access channel II) for the OEM user who also uses the devices attached to the 1133.

The devices that attach to the 1133 are:

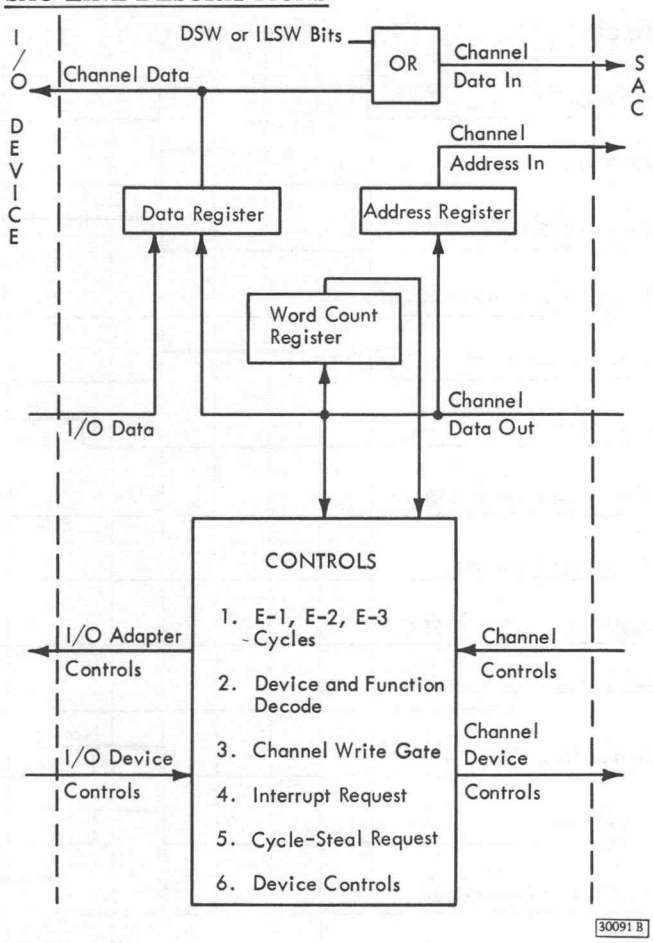
Up to four 2310 Model B Disk Storage access mechanisms.
One 1403 Printer.

The multiplexer, with the 1133, provides signal powering, timing levels, E-cycle levels, core storage addressing facilities, and a cycle-steal request priority scheme for the IBM devices attached to it.

The OEM user must provide functions similar to those provided by the 1133 multiplexer in order to successfully attach a device to the storage access channel. The one exception is that a cycle-steal priority scheme is not necessary if only one device is attached to the SAC.

The 1133 controls are shown in the following diagram:

SAC LINE DESCRIPTIONS



Typical SAC Applications

A wide range of input/output media can be used with the SAC to extend the usefulness of the 1130 system. Typical attachments of input/output media would include:

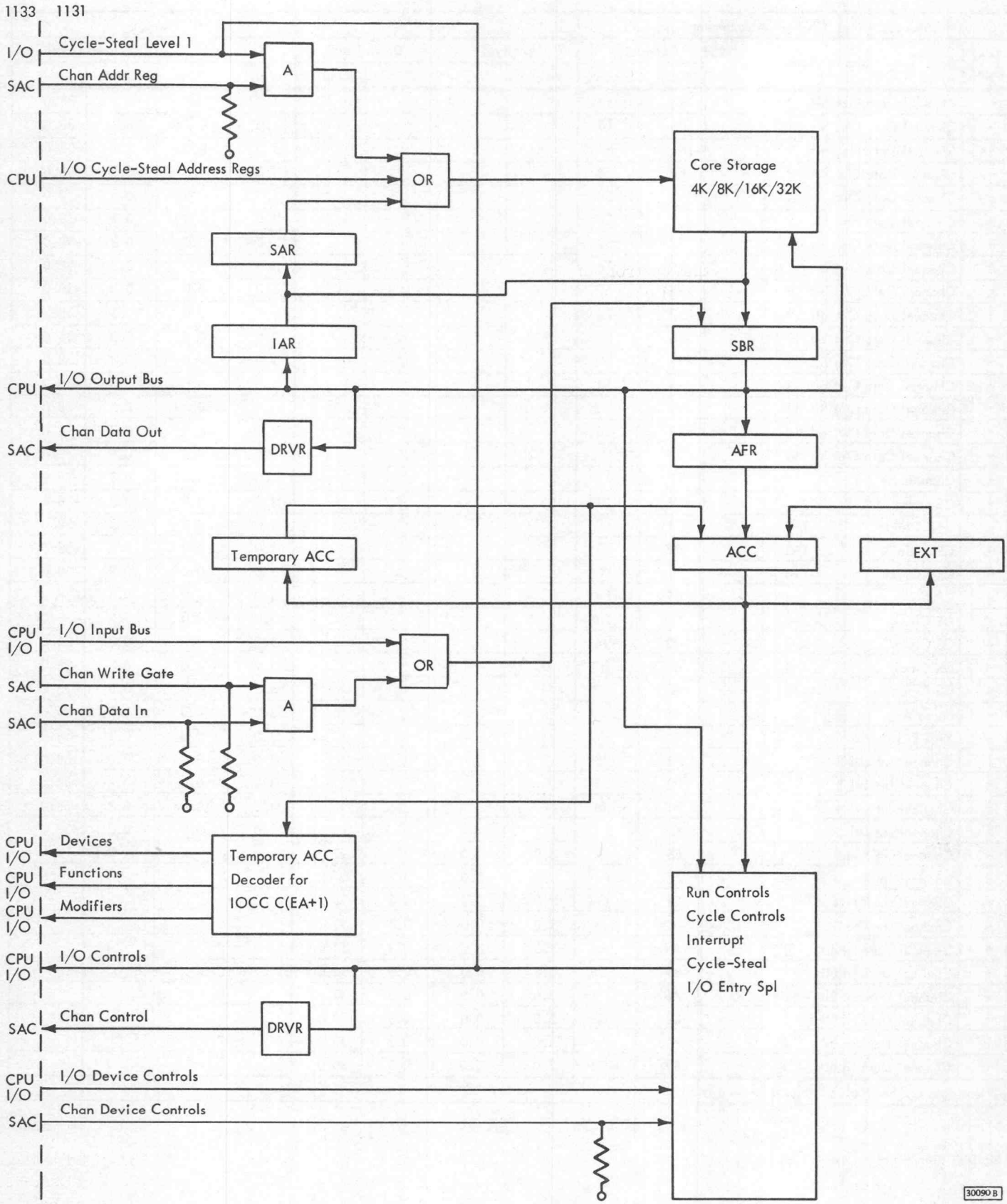
Spectrometers.
Chromatographs.
CRT displays.

or in general:

Monitoring of devices, instruments, or systems.
Control of devices, instruments, or systems.

Storage Access Channel Attachment Points

The attachment points are shown in Figure 8. The lines that connect to these points are described in the section entitled "Storage Access Channel Line Descriptions." The attachment points are the same for both SAC I and SAC II.



● Figure 7. CPU - Interface to SAC and Standard I/O

Storage Access Channel Attachment Point				Input				Output			
True Cond	Signal Name	Connector		Up Level		Down Level		Up Level		Down Level	
		Signal	Ground	Volt*	Ma	Volt*	Ma	Volt*	Ma	Volt*	Ma
-	Channel Data Out Bit 0	R3	S7					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 1	R8	T3					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 2	P6	S1					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 3	R2	S6					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 4	R4	S8					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 5	R9	T4					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 6	P7	S2					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 7	T5	T6					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 8	R5	S9					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 9	T7	T8					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 10	P8	S3					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 11	T9	V1					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 12	R6	T1					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 13	V3	V2					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 14	P9	S4					3.0	0.0	0.3	-38.0
-	Channel Data Out Bit 15	V5	V4					3.0	0.0	0.3	-38.0
-	Chan Reset	R7	T2					3.0	0.0	0.3	-38.0
-	CS Level 1	V6	V7					3.0	0.0	0.3	-38.0
-	CPU Clock T-0	E5	F9					3.0	0.0	0.3	-38.0
-	CPU Clock T-2	D8	F3					3.0	0.0	0.3	-38.0
-	CPU Clock T-4	E6	G1					3.0	0.0	0.3	-38.0
-	CPU Clock T-6	D9	F4					3.0	0.0	0.3	-38.0
-	CS Clock X-0	G5	H8					3.0	0.0	0.3	-38.0
-	CS Clock X-2	H3	J4					3.0	0.0	0.3	-38.0
-	CS Clock X-4	G6	H9					3.0	0.0	0.3	-38.0
-	CS Clock X-6	G7	H4					3.0	0.0	0.3	-38.0
-	Phase A	E7	G2					3.0	0.0	0.3	-38.0
-	XIO E-1 Cycle	G8	H5					3.0	0.0	0.3	-38.0
+	Channel Int Lvl 2	H6	J5					3.0	0.0	0.3	-38.0
+	Channel Int Lvl 3	H1	J2					3.0	0.0	0.3	-38.0
+	Channel Int Lvl 4	H7	J6					3.0	0.0	0.3	-38.0
+	Channel Int Lvl 5	K2	L1					3.0	0.0	0.3	-38.0
-	Channel Int Req 2	E8	G3	3.0	0.0	0.3	30.0				
-	Channel Int Req 3	E2	F6	3.0	0.0	0.3	30.0				
-	Channel Int Req 4	E9	G4	3.0	0.0	0.3	30.0				
-	Channel Int Req 5	H2	J3	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 0	A1	A4	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 1	B1	C5	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 2	A3	A6	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 3	B8	D3	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 4	A2	A5	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 5	B2	C6	3.0	0.0	0.3	30.0				

*Voltages are nominal; voltage tolerance is ±4%.

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Figure 8. Storage Access Channel (part 1 of 2)

Storage Access Channel Attachment Point				Input				Output			
True Cond	Signal Name	Connector		Up Level		Down Level		Up Level		Down Level	
		Signal	Ground	Volt*	Ma	Volt*	Ma	Volt*	Ma	Volt*	Ma
+	Channel Data In Bit 6	B4	C8	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 7	B9	D4	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 8	A7	C2	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 9	B3	C7	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 10	B5	C9	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 11	C1	D5	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 12	A8	C3	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 13	E3	F7	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 14	B6	D1	3.0	0.0	0.3	30.0				
+	Channel Data In Bit 15	D6	F1	3.0	0.0	0.3	30.0				
-	Channel Write Gate	B7	D2	3.0	0.0	0.3	30.0				
-	Block Clock Adv	E4	F8	3.0	0.0	0.3	30.0				
-	Channel CS Req	D7	F2	3.0	0.0	0.3	30.0				
+	Channel Address Bit 0	J7	K6	3.0	0.0	0.3	30.0				
+	Channel Address Bit 1	L8	N3	3.0	0.0	0.3	30.0				
+	Channel Address Bit 2	K3	L2	3.0	0.0	0.3	30.0				
+	Channel Address Bit 3	M6	P1	3.0	0.0	0.3	30.0				
+	Channel Address Bit 4	J8	K7	3.0	0.0	0.3	30.0				
+	Channel Address Bit 5	L9	N4	3.0	0.0	0.3	30.0				
+	Channel Address Bit 6	J9	K8	3.0	0.0	0.3	30.0				
+	Channel Address Bit 7	M7	P2	3.0	0.0	0.3	30.0				
+	Channel Address Bit 8	K4	L5	3.0	0.0	0.3	30.0				
+	Channel Address Bit 9	M1	N5	3.0	0.0	0.3	30.0				
+	Channel Address Bit 10	K1	K9	3.0	0.0	0.3	30.0				
+	Channel Address Bit 11	M8	P3	3.0	0.0	0.3	30.0				
+	Channel Address Bit 12	K5	L6	3.0	0.0	0.3	30.0				
+	Channel Address Bit 13	M2	N6	3.0	0.0	0.3	30.0				
+	Channel Address Bit 14	M4	N8	3.0	0.0	0.3	30.0				
+	Channel Address Bit 15	M9	P4	3.0	0.0	0.3	30.0				
-	Meter Out	E1	F5					3.0	0.0	0.3	-38.0
+	CPU Parity Stop	G9	J1					3.0	0.0	0.3	-38.0
	Spare	A9	C4								
-	Meter In	L7	N2	3.0	0.0	0.3	30.0				
-	Clock Out	M5	N9					3.0	0.0	0.3	-38.0
	Spare	M3	N7								
	Spare	N1	P5								
-	Inhibit CS Request	R1	S5					3.0	0.0	0.3	-38.0

*Voltages are nominal; voltage tolerance is ±4%

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● Figure 8. Storage Access Channel (part 2 of 2)

STORAGE ACCESS CHANNEL LINE DESCRIPTIONS

Channel Data Out: (16 lines) This bus is a data exit from the SBR and reflects the content of the SBR at all times. These lines are stable from T3 or X3 to the fall of T7 or X7, and should be interrogated at all XIO E-1 cycles. (See "XIO E-1 Cycle.")

Channel Reset (DC Reset): This signal results from power-on reset or operation of the console reset key.

Cycle-Steal Level 1: This signal indicates that a CPU cycle-steal level 1 is in progress; the CPU cycle-steal clock (X-clock) runs.

CPU cycle-steal level 1, which is used for SAC I, is ANDed with multiplex level 6 for SAC II. Cycle-steal level 1 is used to gate data to and from the CPU and to gate SAC I and SAC II addresses to the CPU.

Due to delays, cycle-steal level 1 may not be stable at the leading edge of X0.

CPU Clock: (Four lines -- T0, T2, T4, and T6) These signals provide timing pulses for synchronization during XIO E-cycle execution. The pulse duration is 275 nanoseconds (nominal) for the 2.2-microsecond core storage and 444 nanoseconds for the 3.4-microsecond core storage.

Cycle-Steal Clock: (Four lines -- X0, X2, X4, and X6). These signals provide timing pulses for synchronization during cycle-steal execution. The duration of these pulses is the same as the duration of the CPU clock pulses.

Phase A (Oscillator): This signal is generated by a crystal-controlled oscillator operating at 2.25 megahertz (models 1 and 2) or at 3.64 megahertz (model 3). It is used to advance the CPU and cycle-steal clocks. The oscillator runs whenever system power is on.

Because of delays, the phase A signal is skewed with respect to clock times. Care should be exercised if phase A is to be combined with a clock time. The phase A is accurate to within 0.05%.

CPU XIO E-1 Cycle: This signal indicates the beginning of the execution phase of an XIO instruction. It remains active until the next T0 for SAC I and SAC II.

Each device must examine the data out bus, during the E-1 cycle, for its area code. If the area code assigned by the user to the device attached to SAC is recognized, then the attachment will need to decode the function and modifier bits for the action to be taken. For area code assignments for IBM devices see "Area" section under "Input/Output Control Command."

The 1133 channel multiplexer uses the E-1 cycle line from the CPU to generate its own E-1 cycle. The multiplexer E-1 cycle comes on at T3 and remains on until the next T0. (See "Channel Multiplexer Timings.")

The CPU XIO E-1 cycle is repowered in the 1133 and driven onto the XIO E-1 cycle line available to SAC II. The other E-cycles generated by the channel multiplexer are not available to SAC II.

Interrupt Level: (Four levels -- 2, 3, 4, and 5) These signals indicate the highest-level interrupt operation currently in progress. They are used by SAC to gate the proper interrupt level status word (ILSW). See "Input/Output Interrupt Operation."

Interrupt Request: (Four levels -- 2, 3, 4, and 5) These lines may be activated by the SAC user to initiate a program interrupt. Under standard interrupt philsophy for the 1130 system, the request is reset by an XIO Sense instruction with reset modifier bit.

Channel Data In: (16 lines) This bus provides data entry to the storage buffer register (SBR). Data transfer from the SAC user to the CPU is controlled by the channel write gate. Timing is shown in Figures 9, 10, 11.

Channel data should be stable at the CPU terminators from E2-T0 to E2-T4 for a sense operation, and from E3-T2 to E3-T4 for a read operation. See "Channel Write Gate" for data-in controls.

Channel Write Gate: This line is used by the SAC to control the gating of bits on the data in bus into the SBR. This line is required on cycle-steal operations (XIO Initiate Read) and program-controlled operations (XIO Read or XIO Sense).

The channel write gate must be controlled as follows:

1. Cycle-Steal Operation (XIO Initiate Read only). Channel write gate should be made active during the time that the user device recognizes cycle-steal level 1.
2. XIO Sense (ILSW or DSW) operation. The channel write gate should be made active so as to provide the data into the SBR within the time limits required for the channel data in bus, E2-T0 to E2-T4.

On a Sense instruction the SBR is loaded at T2. Some SAC II users may not get channel write gate up in time. In such cases channel write gate and the sense data should be brought up during the E-1 cycle; but also be aware of the exposure in Example 1 below.

3. XIO Read Operation. The channel write gate should be made active so as to provide the data into the SBR during the CPU time interval E3-T2 to E3-T4.

Note: Since the channel write gate is used for data transfer into the SBR, circuits must be provided to insure that data in the SBR is not destroyed if two SAC operations try to overlap. The preceding procedures (1, 2, and 3) must be followed in designing the user's attachment to insure data integrity.

Two hypothetical examples are given next to illustrate the possible misuse of the channel write gate.

Example 1.

Assume that the SAC is transferring data to the CPU using interrupt operation (direct program control, either the XIO Read or an XIO Sense command). Also assume that the channel write gate is activated, by a SAC device, during the E-1 cycle. Suppose that, because of a previous XIO Initiate Write command, the SAC steals the next cycle to transfer data from core storage. Now, since the channel write gate is active (for the Read or Sense) and the SAC recognizes its cycle-steal, the interrupting data will be loaded into the SBR, by mistake, at X3 time of the cycle-steal, thus destroying the cycle-steal data.

The XIO Sense command example is illustrated in Figure 12.

Example 2.

Assume that a system device (not requiring channel write gate) is interrupting sense data into core storage, and that a SAC cycle-steal request comes up just after E2-T0. Suppose that the SAC user's device activates the channel write gate at this time. Now, since the channel write gate is active, whatever is on the data in bus is loaded into the SBR along with the data from the system device that was interrupting, thus destroying the desired data. The same condition could exist for read data, but during the E-3 cycle instead of the E-2 cycle.

Block Clock Advance: This line may be used by the SAC to inhibit advance of the cycle-steal clock during a channel cycle-steal operation. The cycle-steal clock can be stopped only at X2 or X7. Care must be used to prevent blocking the cycle-steal clock while another device is also cycle-stealing, because data from or to that device may be lost. Also, if the X-clock is stopped at X2, the same address must be used for the completion of the cycle.

To stop the cycle-steal clock at X2, block clock advance must be at the CPU terminator no sooner than X0 and no later than the leading edge of X2.

To stop the cycle-steal clock at X7, block clock advance must be at the CPU terminator no sooner than X4 and no later than the leading edge of X7.

No cycle-steal device may be overlapped if the X-clock is blocked at X2. Only the resident disk storage drive may be overlapped if the X-clock is blocked at X7.

A SAC cycle-steal automatically blocks lower level cycle-steal operations for the duration of the SAC cycle-steal.

Channel Cycle-Steal Request: This line is used by SAC to initiate a cycle-steal operation.

SAC I Attachment: The cycle-steal priority is set in the CPU at T7-X7-phase B time. To insure the next cycle is a cycle-steal, this request must be at the CPU terminator no later than the leading edge of T7 or X7. This request should be turned off no later than X6 time of the cycle which is honoring it in order to avoid a second request and to avoid getting two consecutive cycles.

SAC II Attachment: To insure that the next cycle is a cycle-steal, this request must be at the 1133 terminator no later than the trailing edge of T4 or X4. Once activated, this request must not be dropped during the following time interval: from the trailing edge of T4 or X4 to the trailing edge of T7 or X7. The request must be turned off no later than the trailing edge of X4 time. If taking more than one cycle, do not drop this line.

Channel Address In: This bus gates in the core storage address for a cycle-steal operation. The channel address is gated by cycle-steal level 1 at the CPU. The address must be stable at the CPU terminators from the leading edge of X0 through X6. The IBM devices on the 1133 increment the cycle-steal address at the fall of X6 on a 3.6-microsecond system or X6 and phase B on a 2.2-microsecond system.

The cycle-steal address is normally presented with the cycle-steal request and maintained thru X6.

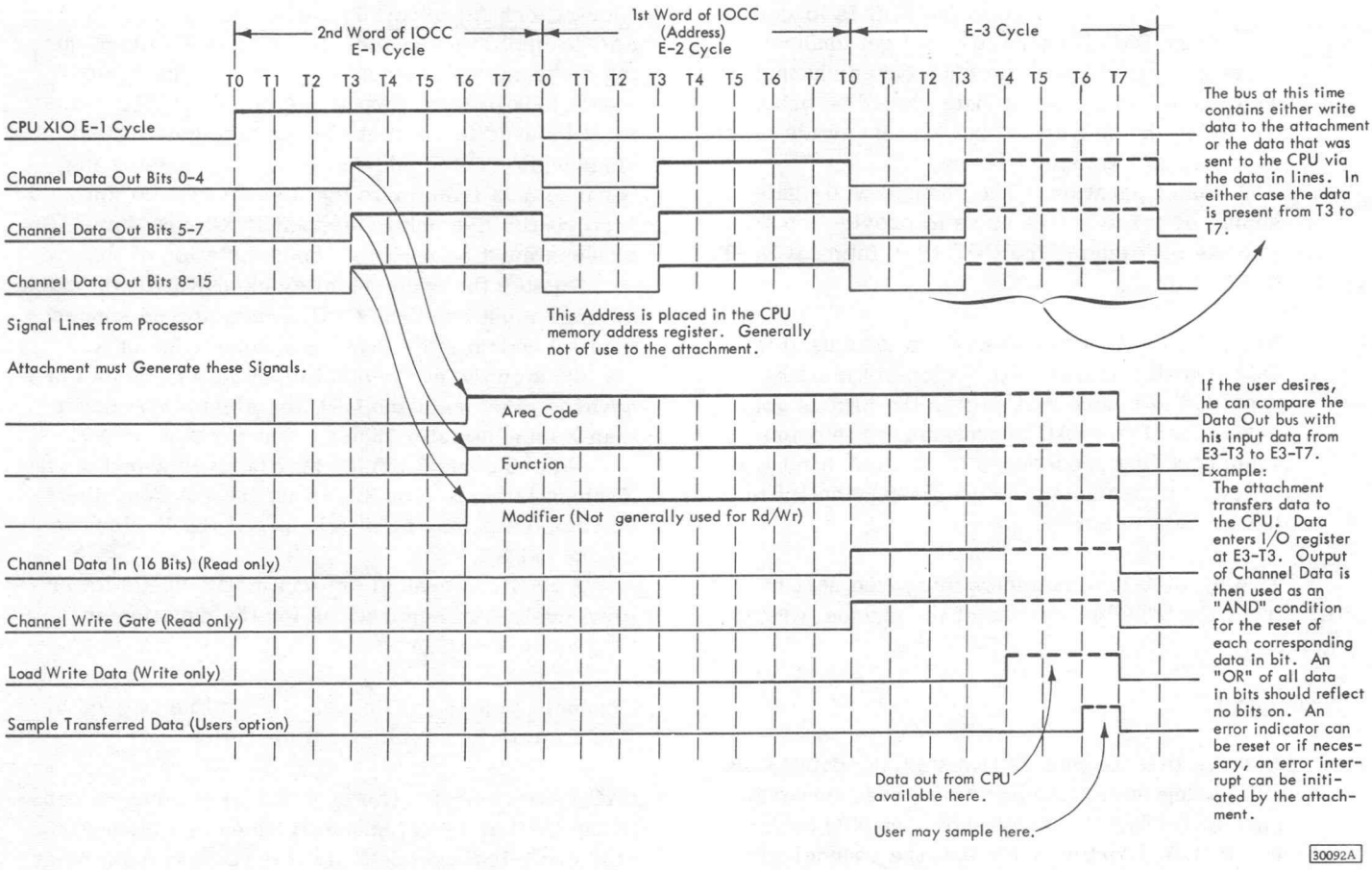


Figure 9. SAC I/O Timing Diagram - XIO Read or Write

For continuous cycle-steals, the address is normally changed after X6 and before X0 of the following cycle. With the additional delays for an OEM device on SAC II, this timing could be critical. For this reason, an additional address register is provided in the 1133 for the OEM user on SAC II. This register holds the contents of the address in lines, from SAC II, from X2 through X6. The OEM user's device can then change the OEM device address any time between X2 and the start of X6.

CPU Meter Out: This signal indicates that the CPU meter is running. It is used to condition the operation of the usage meters of external devices.

CPU Meter In: This line indicates that a device is completing its operation after receiving a CPU instruction. It is used to condition the CPU usage meter for operation in accordance with IBM usage metering policy.

CPU Clock Out: This signal indicates that the CPU clock is running (T- or X-clock). It is used to gate the enable/disable switches on the system. Before any device can change status (e.g., enable or disable) this signal must not be active.

CPU Parity Stop: This signal indicates that the CPU has detected a parity error and halted.

Inhibit Cycle-Steal Request: This line should be used by the OEM device to inhibit the channel cycle-steal request in instances where the percentage of CPU cycles used by the SAC device is such that lower priority devices may be pre-empted enough to cause loss of data.

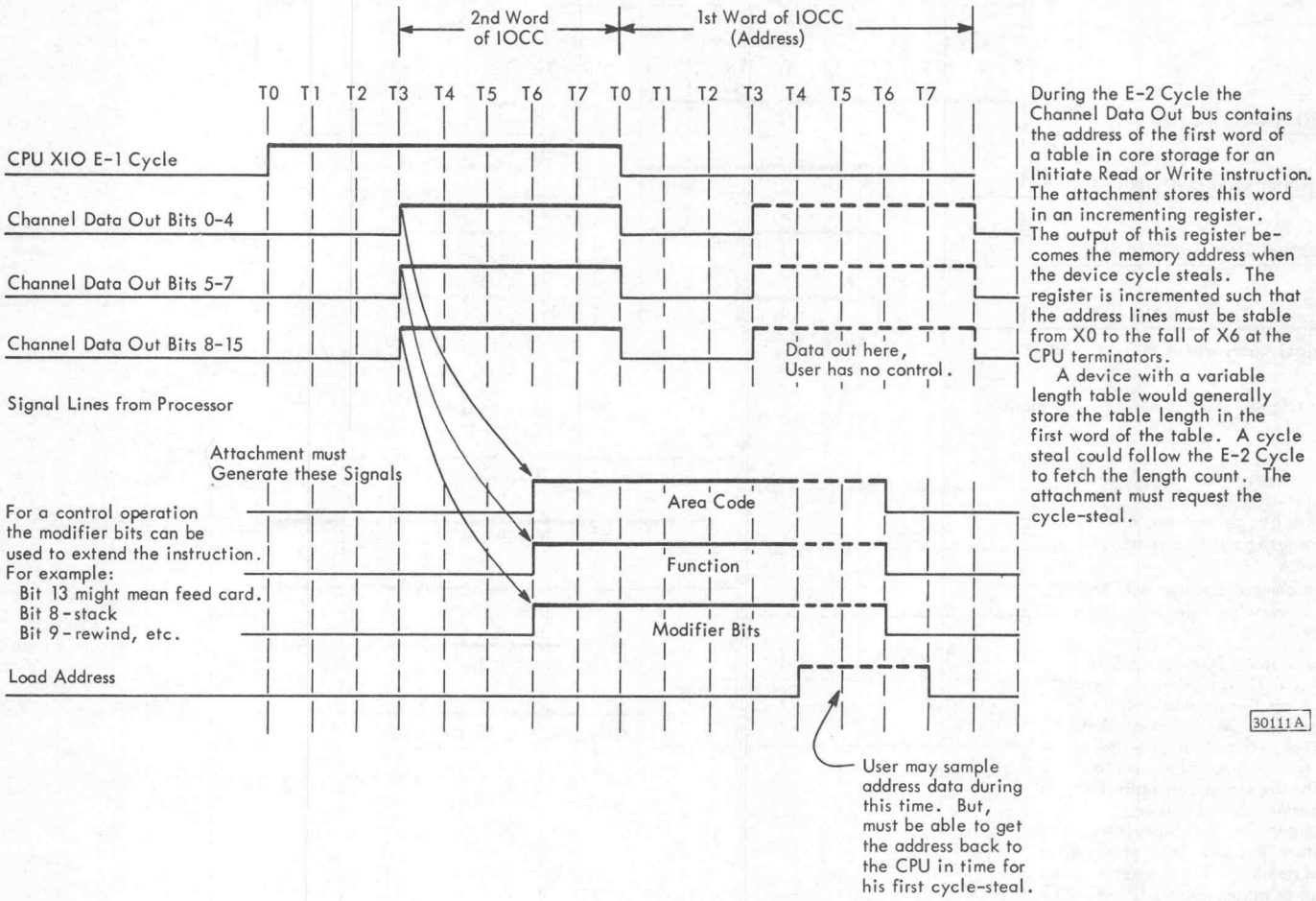


Figure 10. SAC I/O Timing Diagram - XIO Control, Initiate Read/Write

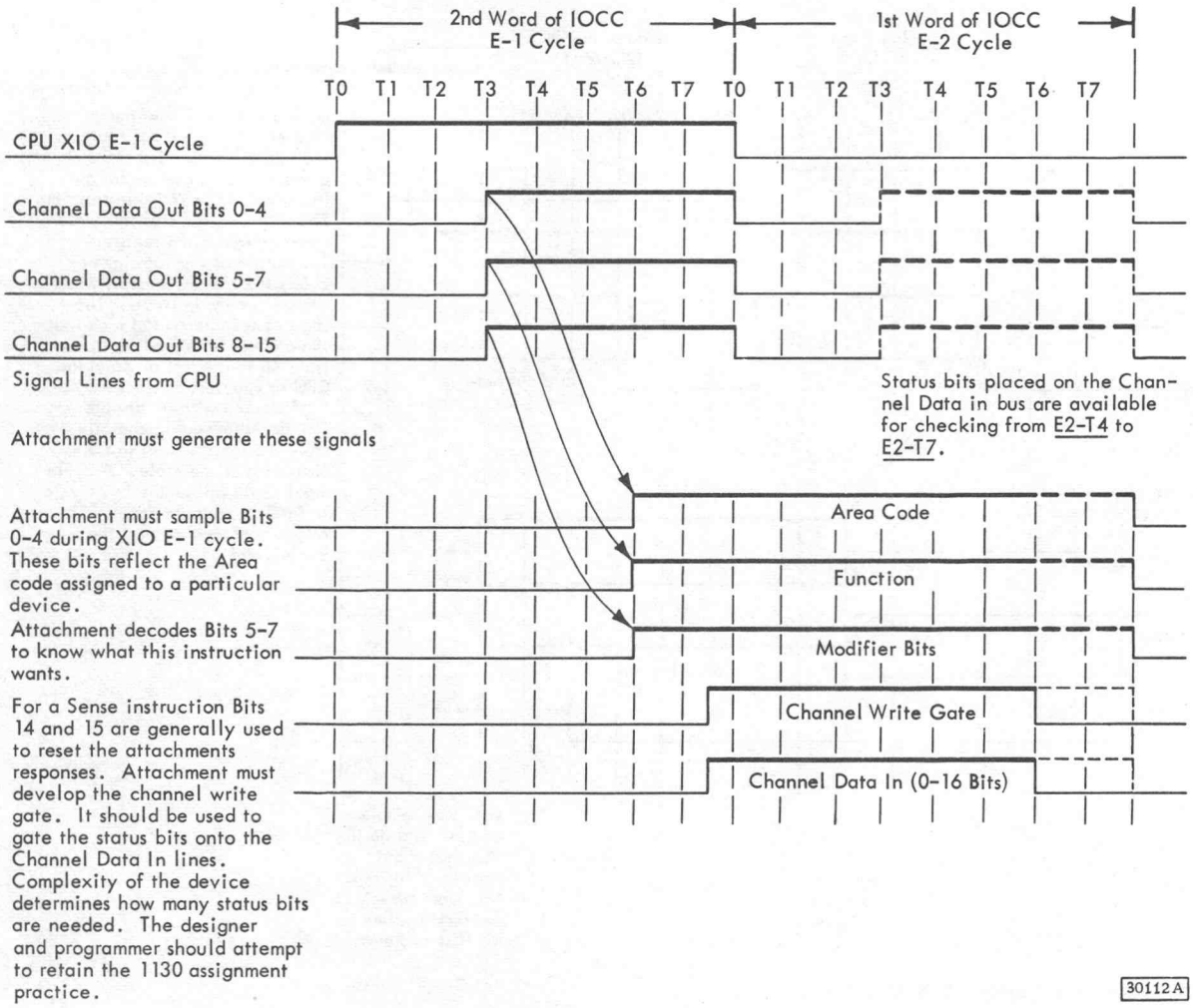
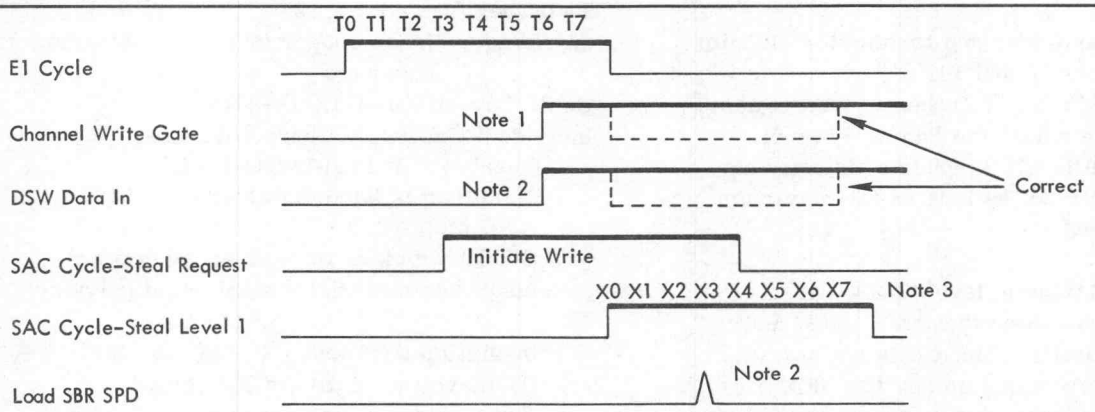


Figure 11. SAC I/O Timing Diagram - XIO Sense

Example 1 - XIO Sense (SAC Device)



Notes:
1. Bringing up Channel Write Gate and data at this time is okay so long as the SAC user does not take the next cycle as a cycle-steal. If the User takes the next cycle, he must drop Channel Write Gate during the Cycle-Steal, but he still must get his sense data to the SBR by E2T0.
2. The load SBR SPD occurred because of Channel Write Gate and Cycle-Steal Level 1. Therefore, the data in the core location that was addressed due to the XIO Initiate Write command was altered by the DSW data at X3 time -- This word is now destroyed! XIO Initiate Write does not use Channel Write Gate.
3. The next cycle will be the E2 cycle unless another cycle-steal occurs.

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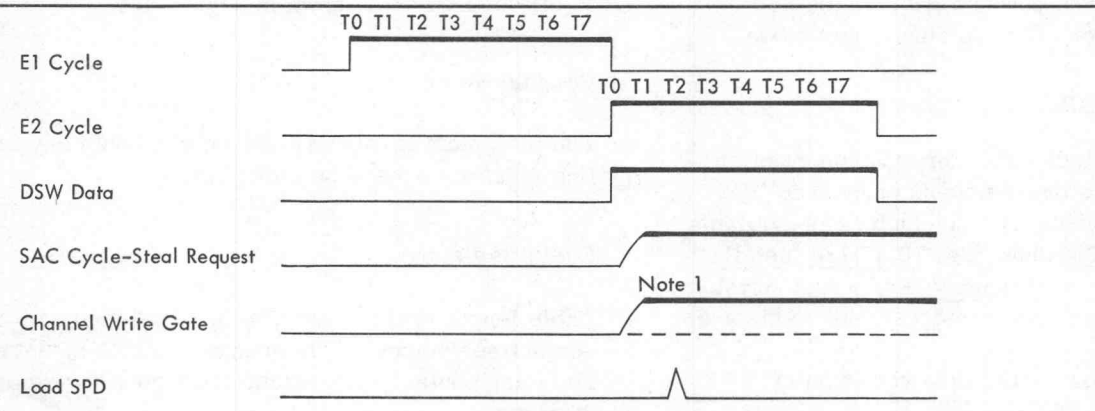
Example 2 - XIO Sense (Non-SAC Device)



Note 1:
Since the Channel Write Gate is active, the data in bus from the SAC device will be loaded into the SBR along with (ORed with) the DSW data. The same condition would exist at the E3 cycle for an XIO Read.

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● Figure 12. Examples of a SAC Device Destroying Data by Improper Control of the Channel Write Gate

Line Drivers and Terminators for SAC

The SAC signal line driver and terminator circuits are shown in Figures 13 and 14.

When the IBM 1133 is attached to these lines, the circuits operate within the "normal" level. However, the circuits will operate efficiently outside of this normal level as long as the maximum levels are not exceeded.

> Note: The maximum levels shown are absolute, which means that noise must not go beyond these limits. Since it is not possible to completely eliminate noise, the OEM user should try to operate at the normal level.

The signal lines to and from these circuits are connected to a 160-pin connector. Each line is made up of a pair of twisted wires. One of the wires in each pair is intended to be a grounded shield and should be tied to ground at both ends.

Power Sequence for SAC Devices

I/O devices attached to the SAC should not be turned on or off while the CPU is processing. To power down a device, the CPU should either be off or in single step mode. To power a device, the CPU should also be either off or in single step mode.

Cabling to OEM Device

The recommended bulk cable for attachment of an OEM device to the storage access channel is IBM part 2158929. (A cable with connectors is available from IBM as part 2243004. See IBM 1130 Installation Manual - Physical Planning (Form A26-5914). Characteristics of the recommended bulk cable are:

Number of conductors = 182 (91 twisted pair)
Cable diameter = 1.16" - 1.24"
Cover type = Polyvinyl chloride 5/64" thick
Twist per foot = 1 ± 0.12"
Shielding = Tinned copper braid for 90% minimum coverage
Cable Lay-up = 1-6-12-18-24-30
Individual Conductor Characteristics:
- Quantity = 182 (91 twisted pair)
- Maximum outside diameter = 0.054"
- AWG size = 22
- Conductor material = stranded copper
- Insulation material = semi-rigid polyvinyl chloride
- Insulation thickness = 0.009" nominal
- U. L. voltage rating = 300 volts
- Temp. rating (insulation) = 80°C, 176°F
- Nominal delay = 2.3 nanoseconds/foot

The external shielding must be connected only to CPU ground through position L3 of the 160-pin receptacle for the SAC.

OEM Attachment

Data, address, and control lines are brought out through a 160-pin receptacle located in the I/O entry area at the rear of the 1131.

The mating plug for quick-disconnect attachment to the 1131 CPU is shown in Figure 15.

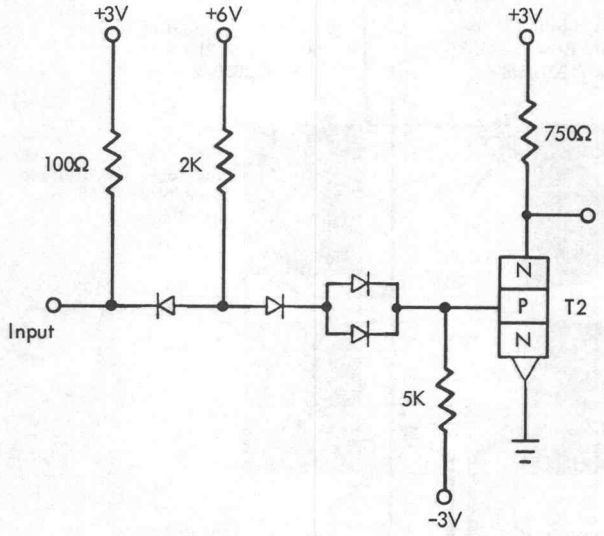
Coupled Noise

The maximum level for noise coupled onto any signal line must not exceed 300 millivolts.

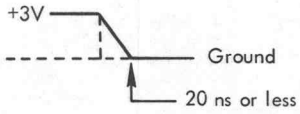
Cable Resistance

Cable length is limited by cable resistance and contact resistance. The maximum cable resistance, including contact resistance, must not exceed 26 ohms.

All input lines from the Storage Access Channel Cable are terminated in the following circuit:



The fall time at the input must be 20 nanoseconds or less to fire T2:



The input specifications for the voltage and current levels are:

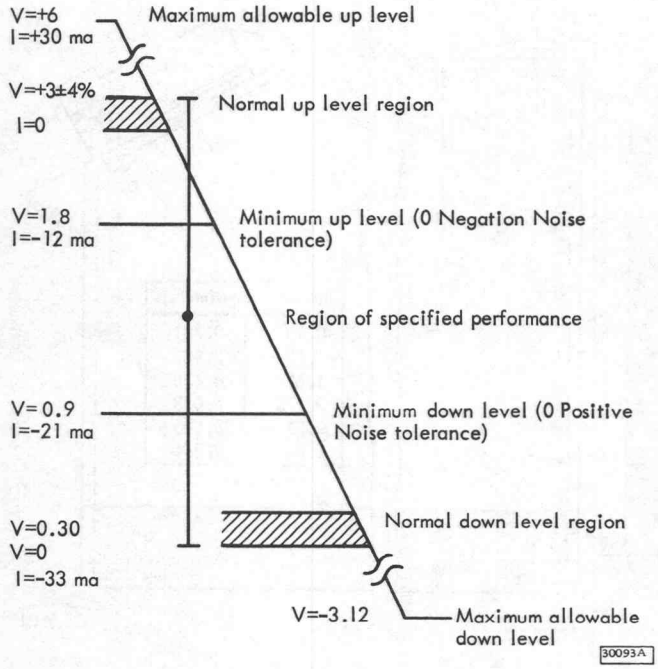
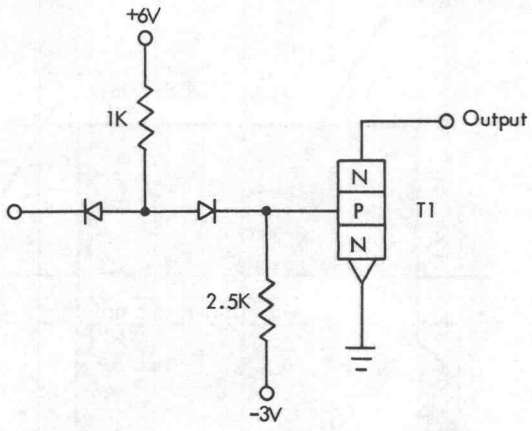


Figure 13. SAC Line Terminator

All output Storage Access Channel Lines are driven by the following circuit:



The output specifications for the voltage and current levels are (as defined by the collector of T1):

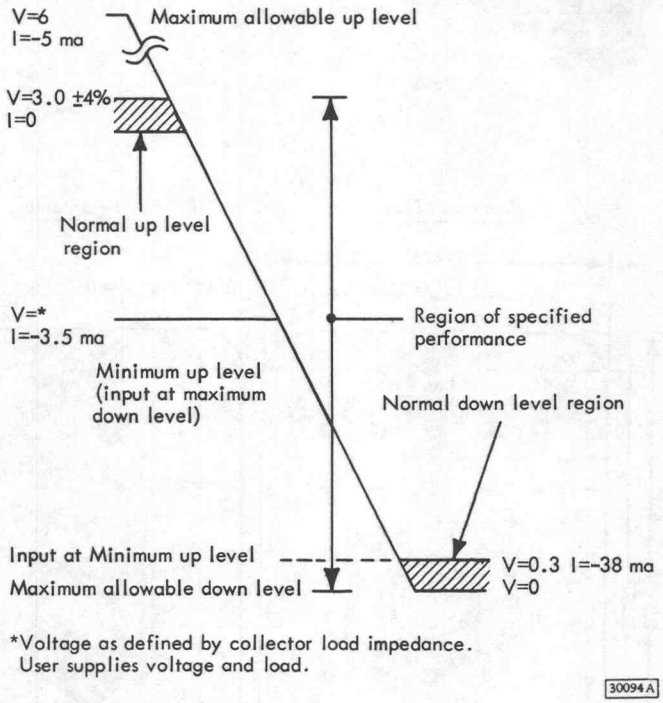
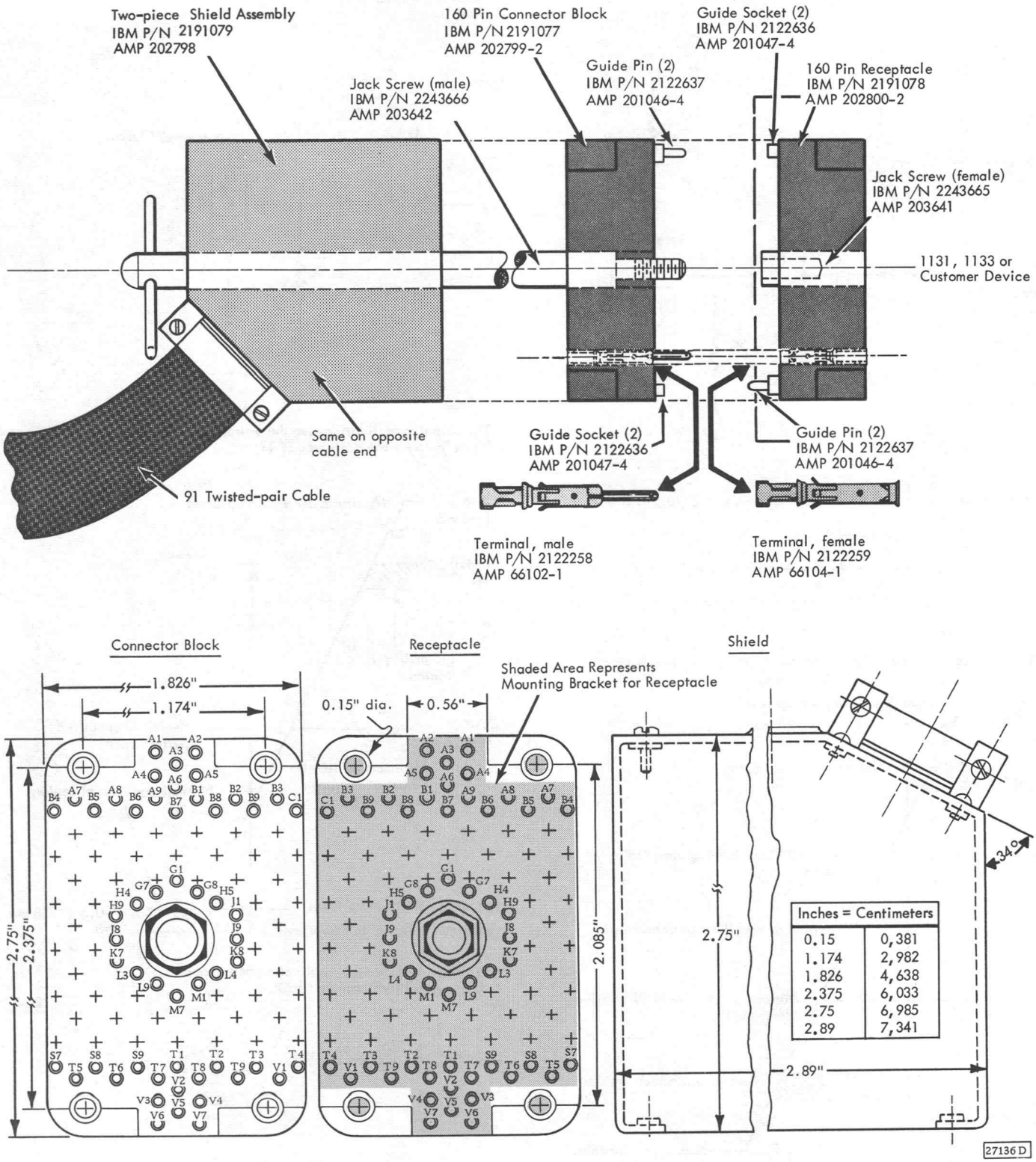


Figure 14. SAC Line Driver



● Figure 15. SAC Cable Connector

ELECTRICAL CHARACTERISTICS

Figure 16 is a summary of the electrical and physical characteristics of the components of the IBM 1130 Computing System.

Electrical Power

Electrical requirements for the IBM 1130 Computing System depend on the system configuration and auxiliary equipment used. (See Figure 16 or 17.)

The voltage and frequency specifications for the 1130 system are:

1. 115vac (±10%); 60Hz (±0.5Hz); single-phase; three-wire (one phase, one neutral, and one grounding conductor).
2. 208 or 230vac (±10%); 60Hz (±0.5Hz); single-phase; three-wire (two phase and one grounding conductor).
3. 208 or 230vac (±10%); 60Hz (±0.5Hz); three-phase; four-wire (three phase and one grounding conductor).
4.* 195, or 220, or 235vac (±10%); 50Hz (±0.5Hz); single-phase; three-wire (one phase, one neutral, and one grounding conductor).
5.* 195, or 220, or 235vac (±10%); 50Hz (±0.5Hz); three-phase; four-wire (three phase and one grounding conductor).

Power Distribution

All power to the 1130 system should be supplied through a single feeder, protected by a mainline circuit breaker. Individual branch circuits from the distribution panel should be protected by circuit breakers suitable for motor load application and derated according to the manufacturer's specifications.

The distribution panel should be located in an unobstructed and well-lighted area within the computer room. As a safety precaution, a remote circuit breaker, which can remove all power from the computer system, should be provided in the machine room.

*Available for use in countries where 50-hertz power distribution systems are used.

Any customer-supplied machine receiving power from the building distribution system should have a branch-circuit protection device. This protection device should be interconnected with the 1130 system mainline circuit breaker, so that all power to machines located in the same room or area can be interrupted from one location under emergency conditions.

Phase Rotation

The three-phase power receptacles for use with the system must be wired for correct phase rotation. Looking at the face of the receptacle, and running counterclockwise from the ground pin, the sequencing will be phase one, phase two, and phase three.

Convenience Outlets

A suitable number of convenience outlets should be installed in the computer room and CE room for use by building maintanance personnel, porter service, Customer Engineers, etc.

Grounding

A green-wire grounding conductor is supplied in each power cord. Each customer-supplied branch circuit should have an insulated wire conductor for the purpose of grounding equipment. All branch-circuit grounding wires can be tied to a common ground point at the distribution panel, and a single grounding wire run from the distribution panel to the nearest grounding station. Conduit must not be used as the only grounding means. Unless otherwise required by local codes, the grounded neutral conductor must be electrically isolated from the system grounding conductor except at the building grounding station.

Lightning Protection

It is recommended that the customer install lightning protection on his secondary power source when any of the following conditions exists:

1. The utility company installs lightning protectors on the primary.

Type	Model	Name	Electrical		Environmental		Weight (lbs.)	Dimensions (inches)			Service Clearances (inches)				Notes
			KVA	Conn. Type*	BTU/Hr	CFM		Width	Depth	Height	F	R	L	Rt	
1131	1A,1B 2A,2B	Central Processing Unit	1.1	B or D	3100	720	660	58.25	29	46.5	42	36	-	30	1,2
1131	2C,2D 3B,3C 3D	Central Processing Unit	1.5	B	4200	1000	1050	88.25	29	46.5	42	36	30	30	1,2
1055	-	Paper Tape Punch	0.06	-	150	-	26	15.375	17.125	8.25	12	12	12	12	3
1132	-	Printer	0.5	-	1300	80	700	47	29.50	42	36	30	30	30	3
1133	-	Multiplex Control Enclosure	1.1	C	3400	500	1100	32	45.50	60	30	30	42	30	
1134	1,2	Paper Tape Punch	0.06	-	150	-	15	19	8.75	8.75	30	12	6	6	3
1231	1	Optical Mark Page Reader	1.2	A	3700	300	620	43.50	24	44.75	42	42	36	30	2
1403	6,7	Printer	1.0	-	2500	310	750	47.75	28.50	53.25	36	36	30	30	4
1442	5	Card Punch	0.7	-	1800	50	525	43	24	49	36	30	18	6	3
1442	6,7	Card Read Punch	0.6	-	1500	50	525	43	24	49	36	30	18	6	3
1627	1	Plotter	0.1	-	250	-	33	18	15	10	12	12	12	12	3
1627	2	Plotter	0.1	-	250	-	55	40	15	10	12	12	12	12	3
2310	B1,B2	Disk Storage	0.7	-	1800	75	365	22	30	44	30	30	24	24	4
2501	A1,A2	Card Reader	0.3	-	700	-	340	30	24	45	36	36	6	24	3

Notes:

1. The base of the Processor is 31.50 inches high, the console adds another 13.50 inches for a total height of 45 inches.
2. This unit is equipped with radio interference control circuitry and requires a good wired earth or building ground. Total resistance of the ground conductor, measured between the receptacle and the building grounding point, must not exceed 3 ohms. For proper operation, all components of the system or systems to which this unit is attached must have the same ground reference. Conduit is not a satisfactory means of grounding.
3. Powered from 1131.
4. Powered from 1133.

* Type	Plug	Connector	Receptacle	Rating	Voltage
A	Russell & Stoll, FS3720	FS3913	FS3743	15 amp, 1 phase, 3 wire	208/230
B	Russell & Stoll, FS3750	FS3933	FS3753	30 amp, 1 phase, 3 wire	208/230
C	Russell & Stoll, FS3760	FS3934	FS3754	30 amp, 3 phase, 4 wire	208/230
D	Hubbell #9338		#9344	30 amp, 1 phase, 3 wire	115

23103F

● Figure 16. Summary of Specifications

Type	Model	Name	Electrical		Environmental		Weight (kg)	Dimensions (Centimeters)			Service Clearances (Centimeters)				Notes
			kva	* Power Cord Style	kcal	m^3/m		Width	Depth	Height	F	R	L	RT	
1131	1A,1B 2A,2B	Central Processing Unit	1.1	A or D	781	20,7	345,7	148	74	115,6	107	91	-	76	1,2, 5,6
1131	2C,2D 3B,3C 3D	Central Processing Unit	1.5	A or D	1058	28,3	477	224	74	115,6	107	91	76	76	1,2,5
1055	-	Paper Tape Punch	0.06	-	37,8	-	16,3	40	44	21	30	30	30	30	3
1132	-	Printer	0.5	-	328	2,26	317,5	119	75	107	91	76	76	76	3
1133	-	Multiplex Control Enclosure	1.1	C	857	14,2	499	81	116	152	76	76	107	76	
1134	1,2	Paper Tape Reader	0.06	-	37,8	-	6,8	48	22	22	76	30	15	15	3
1231	1	Optical Mark Page Reader	1.2	A	932	8,49	281	110	61	114	107	107	91	76	2
1403	6,7	Printer	1.0	-	630	8,77	340	121	72	135	91	91	76	76	4
1442	5	Card Punch	0.7	-	454	1,42	238	109	61	124	91	76	46	15	3
1442	6,7	Card Read Punch	0.7	-	454	1,42	238	109	61	124	91	76	46	15	3
1627	1	Plotter	0.1	-	63	-	15	46	38	2,5	30	30	30	30	3
1627	2	Plotter	0.1	-	63	-	24,9	102	38	2,5	30	30	30	30	3
2310	B1,B2	Disk Storage	0.7	-	454	2,12	165	56	76	112	76	76	61	61	4
2501	A1,A2	Card Reader	0.3	-	17,6	-	154	76	61	114	91	91	15	61	3
2250	4	Display Unit	1.0	E or F	756	11,9	272	149	164	127	76	25	102	76	5

Notes:

1. The base of the Processor is 80 centimeters high, the console adds another 35,6 centimeters for a total height of 115,6.
2. This unit is equipped with radio interference control circuitry and requires a good wired earth or building around. Total resistance of the ground conductor, measured between the receptacle and the building grounding point, must not exceed 3 ohms. For proper operation, all components of the system or systems to which this unit is attached must have the same ground reference. Conduit is not a satisfactory means of grounding.
3. Powered from 1131.
4. Powered from 1133.
5. Power is supplied by the 1133 if installed.
6. If a 1231, 1442-5 or a 2501 is installed the 1131 must be 195, 220 or 235 vac.
7. All 115-volt machines are equipped with Hubbell (#9338) plugs. All 115-volt machines shipped after January 1, 1968, will be equipped with Arrow Hart (#5717) plugs.

* Power Cord Style	Cable			Conductors				Insulation					Branch Circuit
	Nominal O.D.		Body Color	Qty	Awg	Shield	Material	Nominal O.D.		Material	Body Color	Volt Rating	
	Inch	cm						Inch	cm				
A. 50 Hz	0.405	1,0	Grey	3	12	None	Stranded Tinned Copper	0.03	0,076	PVC	Note 1	Note 2	15 amp, 1Ø, 3 wire
C. 50 Hz *	0.750	1,9	"	5	10	Yes	"	0.094	0,24	"	Note 3	600	30 amp, 3Ø, 5 wire
D. 50 Hz #	0.405	1,0	"	3	12	None	"	0.03	0,076	"	Note 4	Note 2	15 amp, 1Ø, 3 wire
E. 50 Hz Note 5	0.58	1,47	"	3	12	Yes	"	0.094	0,24	"	Note 1	600	20 amp, 1Ø, 3 wire
F. 50 Hz# Note 5	0.58	1,47	"	3	12	Yes	"	0.094	0,24	"	Note 4	600	20 amp, 1Ø, 3 wire

* For countries using 50 Hertz power.
# United Kingdom.

Notes:

1. Green/Yellow for Lead 1. Blue for Lead 2. Black for Lead 3.
2. Ground to any conductor, 250 volts. Between any two conductors, 500 volts.
3. Black for Leads 1, 2 and 3. Blue for Lead 4. Green/Yellow for Lead 5.
4. Green/Yellow for Lead 1. Black for Lead 2. Red for Lead 3.
5. An external flexible steel conduit 0.75" I.D. (1,9 cm) covers the attachment cord. This is grounded at the 2250 end, and must also be grounded at the receptacle end.

27077G

● Figure 17. Summary of Specifications (Metric)

2. Primary power is supplied by an overhead power service.
3. The area is subject to electrical storms or equivalent power surges.

ENVIRONMENTAL REQUIREMENTS

Ambient Air Conditions

All IBM 1130 Computing Systems use air for internal cooling. Cool air is introduced through the bottom or side of each unit, internally circulated by fans or natural convection, and exhausted to the room from the top. The following limits should be maintained for ambient air to ensure normal operation of the system:

Temperature: 60° F to 90° F
Relative humidity: 10% to 80%
Maximum wet bulb temperature: 78° F

Dust and Dirt Control

The amount of contamination in the office atmosphere will not normally interfere with the operation of the 1130 system. Normal precautions should be taken, however, to keep dust, dirt, and other foreign matter away from the machine area.

Fire Protection Equipment

Portable carbon-dioxide fire extinguishers of suitable size should be provided in the computing system area, subject to local building-code and fire-insurance requirements. A nonwetting fire-extinguishing agent for electrical equipment (Class C hazard) is recommended.

IBM I/O DEVICE ATTACHMENT POINTS

The attachment points for the IBM devices available for the 1130 system are listed in this section. This section also includes I/O power and signal connectors.

The following attachment points are listed as follows:

For attachment to the 1131

IBM 1134 Paper Tape Reader, Figure 18.
IBM 1055 Paper Tape Punch, Figure 19.
IBM 1132 Printer, Figure 20.
IBM 1442 Card Read Punch, Figure 21.
IBM 1627 Plotter, Figure 22.
IBM 2501 Card Reader, Figure 23.
IBM 1231 Optical Mark Page Reader, Figure 24.

For attachment to the 1133

IBM 1403 Printer, Figure 25.
IBM 2310 Model B Disk Storage (first drive only), Figure 26.

The four attachments for the four 2310 Disk Drives are identical in function. For this reason, only the first drive attachment points are listed.

I/O Adapters

The function of an I/O adapter is to provide the logical interface for operating and controlling attached I/O devices. The interface for IBM devices are designed so that no adapter can block the transmission signals or controls to another adapter. However, the block clock advance provided for the storage access channel will stop the CPU clock and, in effect, block all other adapters.

The I/O adapter in the 1131 CPU decodes commands received from the CPU, interprets them for each device attached to the CPU (except for devices attached through SAC), and provides the operating sequence required for proper execution. It also adapts the characteristics of each device to an information format and signal sequence common to the CPU.

Each I/O device has an adapter, and only one adapter per instruction can be selected to communicate with the CPU. An adapter is selected by an instruction generated by the CPU program.

Electrical Considerations

Transmission Lines

Transmission lines used with the 1131 and the 1133 can be driven by single drivers and can feed single receivers. All transmission lines must have a characteristic impedance of 95 ohms (±10 ohms).

IBM 1134 Attachment Point			Input				Output			
True Cond	Signal Name	Connector	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
-	Gate P.T. Read Contacts Common	PF3-J	3.0	0.0	0.33	31.2				
-	P.T. Read Contact C	PF3-K	3.0	0.0	0.33	31.2				
-	P.T. Read Contact 1	PF3-L	3.0	0.0	0.33	31.2				
-	P.T. Read Contact 2	PF3-M	3.0	0.0	0.33	31.2				
-	P.T. Read Contact 4	PF3-N	3.0	0.0	0.33	31.2				
-	P.T. Read Contact 8	PF3-P	3.0	0.0	0.33	31.2				
-	P.T. Read Contact A	PF3-Q	3.0	0.0	0.33	31.2				
-	P.T. Read Contact B	PF3-R	3.0	0.0	0.33	31.2				
-	P.T. Read Contact 8th Chan	PF3-C	3.0	0.0	0.33	31.2				
-	P.T. Reader Ready	PF3-B	3.0	0.0	0.30	4.6				
-	P.T. Reader Clutch Drive B	PF3-A					48.0	NA	0.7	-300.0
-	P.T. Reader Clutch Drive A	PF3-F					48.0	NA	0.7	-300.0

11400 B

Figure 18. 1134 Paper Tape Reader

IBM 1055 Attachment Point			Input				Output			
True Cond	Signal Name	Connector	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
-	Drive P.T. Punch Clutch	PF5-F					48.0	NA	0.7	-300.0
-	P.T. Punch 8th Chan Drive	PF5-G					48.0	NA	0.7	-300.0
-	P.T. Punch C Drive	PF5-K					48.0	NA	0.7	-300.0
-	P.T. Punch 1 Drive	PF5-L					48.0	NA	0.7	-300.0
-	P.T. Punch 2 Drive	PF5-M					48.0	NA	0.7	-300.0
-	P.T. Punch 4 Drive	PF5-N					48.0	NA	0.7	-300.0
-	P.T. Punch 8 Drive	PF5-P					48.0	NA	0.7	-300.0
-	P.T. Punch A Drive	PF5-Q					48.0	NA	0.7	-300.0
-	P.T. Punch B Drive	PF5-R					48.0	NA	0.7	-300.0
-	P.T. Punch Ready	PF5-H	3.0	0.0	0.3	4.6				

11401B

Figure 19. 1055 Paper Tape Punch

IBM 1132 Attachment Point			Input				Output			
True Cond	Signal Name	Connector	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
+	Print Disc Bit 0	PC7N9	3.0	0.0	0.3	2.3				
+	Print Disc Bit 1	PC7N8	3.0	0.0	0.3	2.3				
+	Print Disc Bit 2	PC7M3	3.0	0.0	0.3	2.3				
+	Print Disc Bit 3	PC7L1	3.0	0.0	0.3	2.3				
+	Print Disc Bit 4	PC7K1	3.0	0.0	0.3	2.3				
+	Print Disc Bit 5	PC7J3	3.0	0.0	0.3	2.3				
+	Print Disc Bit 6	PC7H1	3.0	0.0	0.3	2.3				
+	Print Disc Bit 7	PC7G9	3.0	0.0	0.3	2.3				
+	Carriage Brush 1	PC7T8	3.0	0.0	0.3	7.6				
+	Carriage Brush 2	PC7T7	3.0	0.0	0.3	5.3				
+	Carriage Brush 3	PC7T6	3.0	0.0	0.3	5.3				
+	Carriage Brush 4	PC7T5	3.0	0.0	0.3	5.3				
+	Carriage Brush 5	PC7P5	3.0	0.0	0.3	5.3				
+	Carriage Brush 6	PC7P4	3.0	0.0	0.3	5.3				
+	Carriage Brush 9	PC7P3	3.0	0.0	0.3	5.3				
+	Carriage Brush 12	PC7P2	3.0	0.0	0.3	5.3				
+	Start Key	PC7T4	3.0	0.0	0.3	4.6				
+	Stop Key	PC7T9	2.0	0.5	0.3	2.3				
+	Forms Contact	PC7R1	3.0	-11.9	0.3	-4.7				
+	Interposer Contact	PC7R2	3.0	-12.8	0.3	-4.7				
+	Print Disc Clock	PC7P1	3.0	0.0	0.3	7.5				
+	Motor On Sw	PC7S8	2.0	0.5	0.3	-2.4				
+	Carriage Stop Sw	PC7S9	2.0	0.5	0.3	0.0				
+	Carriage Restore Sw	PC7T1	3.0	0.0	0.3	5.3				
-	Carriage CB	PC7S7	2.0	0.5	0.3	0.0				
+	Carriage Space Sw	PC7T2	3.0	0.0	0.3	2.3				
+	Space Interrupt Allow	PC7P9	3.0	0.0	0.3	-14.8				

11409 C

Figure 20. 1132 Printer (part 1 of 2)

IBM 1132 Attachment Point			Input				Output			
True Cond	Signal Name	Connector	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
+	Print Select Group 0	PC7J7					3.0	0.0	0.3	-37.4
+	Print Select Group 1	PC7G4					3.0	0.0	0.3	-37.4
+	Print Select Group 2	PC7G3					3.0	0.0	0.3	-37.4
+	Print Select Group 3	PC7G2					3.0	0.0	0.3	-37.4
+	Print Select Group 4	PC7C9					3.0	0.0	0.3	-37.4
+	Print Select Group 5	PC7C8					3.0	0.0	0.3	-37.4
+	Print Select Group 6	PC7D7					3.0	0.0	0.3	-37.4
+	Print Select Group 7	PC7D6					3.0	0.0	0.3	-32.8
+	Print Buffer 0	PC7G7					3.0	0.0	0.3	-21.0
+	Print Buffer 1	PC7G1					3.0	0.0	0.3	-21.0
+	Print Buffer 2	PC7G6					3.0	0.0	0.3	-21.0
+	Print Buffer 3	PC7F9					3.0	0.0	0.3	-21.0
+	Print Buffer 4	PC7G5					3.0	0.0	0.3	-21.0
+	Print Buffer 5	PC7F8					3.0	0.0	0.3	-21.0
+	Print Buffer 6	PC7D5					3.0	0.0	0.3	-21.0
+	Print Buffer 7	PC7F7					3.0	0.0	0.3	-21.0
+	Print Buffer 8	PC7D4					3.0	0.0	0.3	-21.0
+	Print Buffer 9	PC7E2					3.0	0.0	0.3	-21.0
+	Print Buffer 10	PC7D3					3.0	0.0	0.3	-21.0
+	Print Buffer 11	PC7E1					3.0	0.0	0.3	-21.0
+	Print Buffer 12	PC7D2					3.0	0.0	0.3	-21.0
+	Print Buffer 13	PC7D9					3.0	0.0	0.3	-21.0
+	Print Buffer 14	PC7D1					3.0	0.0	0.3	-21.0
+	Print Buffer 15	PC7D8					3.0	0.0	0.3	-21.0
-	Carriage Mag Select	PC7L7					3.0	0.0	0.3	-14.8
-	Forms Indicator	PC7P8					3.0	0.0	0.3	-14.8
-	Print Scan Error	PC7P7					3.0	0.0	0.3	-14.8
-	Motor On Indicator	PC7P6					3.0	0.0	0.3	-14.8
-	Ready Indicator	PC7L6					3.0	0.0	0.3	-14.8
-	Interposer Mag Select	PC7J6					3.0	0.0	0.3	-14.8
-	Use Meter Select	PC7T3					3.0	0.0	0.3	-14.8
+	Print Gate	PC7G8					3.0	0.0	0.3	-14.8

11410C

Figure 20. 1132 Printer (part 2 of 2)

IBM 1442 Attachment Point				Input				Output			
True Cond	Signal Name		Connector	Up Level		Down Level		Up Level		Down Level	
				Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
-	Punch Magnet	12	PC6J4					3.0	0.0	0.3	-15.0
-	Punch Magnet	11	PC6J9					3.0	0.0	0.3	-15.0
-	Punch Magnet	0	PC6J3					3.0	0.0	0.3	-15.0
-	Punch Magnet	1	PC6J8					3.0	0.0	0.3	-15.0
-	Punch Magnet	2	PC6H1					3.0	0.0	0.3	-15.0
-	Punch Magnet	3	PC6G4					3.0	0.0	0.3	-15.0
-	Punch Magnet	4	PC6G8					3.0	0.0	0.3	-15.0
-	Punch Magnet	5	PC6G3					3.0	0.0	0.3	-15.0
-	Punch Magnet	6	PC6G7					3.0	0.0	0.3	-15.0
-	Punch Magnet	7	PC6G2					3.0	0.0	0.3	-15.0
-	Punch Magnet	8	PC6G6					3.0	0.0	0.3	-15.0
-	Punch Magnet	9	PC6F9					3.0	0.0	0.3	-15.0
+	Incr Drive A		PC6A5					3.0	0.0	0.3	-21.0
+	Incr Drive B		PC6A6					3.0	0.0	0.3	-21.0
+	SRP Feed Clutch		PC6D6					3.0	0.0	0.3	-14.8
-	Motor Relay		PC6C8					3.0	0.0	0.3	-14.8
+	SRP Ready Powered		PC6G5					3.0	0.0	0.3	-24.0
+	SRP Error		PC6F8					3.0	0.0	0.3	-15.0
+	Mis-Feed		PC6E2					3.0	0.0	0.3	-14.8
+	Punch Error		PC6D3					3.0	0.0	0.3	-21.0
+	Feed Check Read Station		PC6F7					3.0	0.0	0.3	-14.8
+	Read Error		PC6D4					3.0	0.0	0.3	-21.0
+	Feed Check Punch Station		PC6E1					3.0	0.0	0.3	-14.8
+	Stacker Transport		PC6D5					3.0	0.0	0.3	-14.8
+	Feed Clutch Mis-Feed		PC6J7					3.0	0.0	0.3	-14.8
-	Stacker Select		PC6C9					3.0	0.0	0.3	-15.0
-	SRP Busy		PC6D8					3.0	0.0	0.3	-15.0
-	SRP Process Meter		PC6D2					3.0	0.0	0.3	-15.0

11402C

Figure 21. 1442 Card Read Punch (part 1 of 2)

IBM 1442 Attachment Point			Input				Output			
True Cond	Signal Name	Connector	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
+	Hopper Empty Switch	PC6L1	3.0	-12.8	0.3	-7.0				
+	NPRO Switch	PC6J6	3.0	-12.8	0.3	-7.0				
+	Start Switch	PC6L7	3.0	-12.8	0.3	-7.0				
-	Stop Switch	PC6L2	3.0	-12.8	0.3	-7.0				
-	Stacker Jam Switch	PC6J5	3.0	-12.8	0.3	-7.0				
-	Idle Relay Contact	PC6K1	3.0	-12.8	0.3	-7.0				
+	Read SCA 12	PC6V5	3.0	0.0	0.3	2.3				
+	Read SCA 11	PC6V7	3.0	0.0	0.3	2.3				
+	Read SCA 0	PC6T4	3.0	0.0	0.3	2.3				
+	Read SCA 1	PC6T3	3.0	0.0	0.3	2.3				
+	Read SCA 2	PC6V6	3.0	0.0	0.3	2.3				
+	Read SCA 3	PC6T2	3.0	0.0	0.3	2.3				
+	Read SCA 4	PC6U1	3.0	0.0	0.3	2.3				
+	Read SCA 5	PC6T9	3.0	0.0	0.3	2.3				
+	Read SCA 6	PC6T1	3.0	0.0	0.3	2.3				
+	Read SCA 7	PC6T8	3.0	0.0	0.3	2.3				
+	Read SCA 8	PC6S9	3.0	0.0	0.3	2.3				
+	Read SCA 9	PC6S8	3.0	0.0	0.3	2.3				
+	Punch Lamp Dark	PC6P7	3.0	0.0	0.3	3.0				
+	Read Emitter	PC6T7	3.0	-12.8	0.3	7.0				
+	Feed CB1	PC6S7	3.0	0.0	0.3	9.5				
+	Punch CB1	PC6P4	3.0	0.0	0.3	9.5				
+	Feed CB2	PC6T6	3.0	0.0	0.3	9.5				
-	Punch CB2	PC6P9	3.0	0.0	0.3	9.5				
+	Feed CB3	PC6R2	3.0	0.0	0.3	9.5				
+	Incr Drive CBA	PC6P3	3.0	0.0	0.3	9.5				
-	Feed CB4	PC6R1	3.0	0.0	0.3	9.5				
-	Incr Drive CBB	PC6P8	3.0	0.0	0.3	9.5				
+	Punch Check Amp 12	PC6P2	3.0	0.0	0.3	3.0				
+	Punch Check Amp 11	PC6P6	3.0	0.0	0.3	3.0				
+	Punch Check Amp 0	PC6P1	3.0	0.0	0.3	3.0				
+	Punch Check Amp 1	PC6N9	3.0	0.0	0.3	3.0				
+	Punch Check Amp 2	PC6L6	3.0	0.0	0.3	3.0				
+	Punch Check Amp 3	PC6N8	3.0	0.0	0.3	3.0				
+	Punch Check Amp 4	PC6L5	3.0	0.0	0.3	3.0				
+	Punch Check Amp 5	PC6L4	3.0	0.0	0.3	3.0				
+	Punch Check Amp 6	PC6M3	3.0	0.0	0.3	3.0				
+	Punch Check Amp 7	PC6L8	3.0	0.0	0.3	3.0				
+	Punch Check Amp 8	PC6M2	3.0	0.0	0.3	3.0				
+	Punch Check Amp 9	PC6L3	3.0	0.0	0.3	3.0				

11403C

Figure 21. 1442 Card Read Punch (part 2 of 2)

IBM 1627 Attachment Point			Input				Output			
True Cond	Signal Name	Connector	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
+	Not Ready	PF6-G	3.0	0.0	0.3	2.0				
-	Pen Down Drive	PF6-L					12.0	NA	0.4	-25.0
-	Pen Up Drive	PF6-M					12.0	NA	0.4	-25.0
-	Carr Left Drive	PF6-N					12.0	NA	0.4	-25.0
-	Carr Right Drive	PF6-P					12.0	NA	0.4	-25.0
-	Drum Down Drive	PF6-Q					12.0	NA	0.4	-25.0
-	Drum Up Drive	PF6-R					12.0	NA	0.4	-25.0

11408C

Figure 22. 1627 Plotter

IBM 2501 Attachment Point			Input				Output			
True Cond	Signal Name	Connector	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
+	Read Cell 12	PC8 L9	3.0		0.3					
+	Read Cell 11	PC8 F3	3.0		0.3					
+	Read Cell 0	PC8 S9	3.0		0.3					
+	Read Cell 1	PC8 L3	3.0		0.3					
+	Read Cell 2	PC8 D1	3.0		0.3					
+	Read Cell 3	PC8 P7	3.0		0.3					
+	Read Cell 4	PC8 J8	3.0		0.3					
+	Read Cell 5	PC8 C4	3.0		0.3					
+	Read Cell 6	PC8 P1	3.0		0.3					
+	Read Cell 7	PC8 F9	3.0		0.3					
+	Read Cell 8	PC8 T6	3.0		0.3					
+	Read Cell 9	PC8 L8	3.0		0.3					
+	Feed CB 1	PC8 T1	3.0		0.3					
+	Feed CB 2	PC8 G1	3.0		0.3					
+	Feed CB 3	PC8 T7	3.0		0.3					
+	Card Lever	PC8 P8	3.0		0.3					
+	Read Emitter	PC8 P2	3.0		0.3					
-	Block Read Emitter	PC8 D2	0.0		NA					
+	Stop Key	PC8 P3	3.0		NA					
+	Start Key	PC8 R1	3.0		NA					
-	NPRO Key	PC8 E1	0.0		NA					
+	Hopper Empty	PC8 M2	3.0		NA					
-	Stacker Full	PC8 G9	0.0		NA					
-	Motor Hold Switch	PC8 T3	3.0		NA					
-	Fiber Optic Test	PC8 P4								
-	Cover Open	PC8M1								
-	Motor Relay	PC8 T8					3.0		0.0	
-	Feed Solenoids	PC8 P9					3.0		0.0	
-	Hopper Magnet	PC8 F4					3.0		0.0	
-	Record Emitter	PC8 D7					3.0		0.0	
-	Erase Emitter	PC8 G6					3.0		0.0	
-	Process Meter Go	PC8 T2					3.0		0.0	
+	Ready Indicator	PC8 L4					3.0		0.0	
+	Read Check Indicator	PC8 G2					3.0		0.0	
+	Attention Indicator	PC8 T9					3.0		0.0	
-	Execute Command	PC8 J5					3.0		0.0	

30096 B

Figure 23. 2501 Card Reader

IBM 1231 Attachment Point			Input				Output			
True Cond	Signal Name	Connector	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
-	Master Mark Buffer Full	PC8 L3	3.0		0.0					
-	Trans 1 Auto Select	PC8 C4	3.0		0.0					
-	I/O Trans 5 Read Error	PC8 D1	3.0		0.0					
-	I/O Trans 6 Timing Mark Check	PC8 P1	3.0		0.0					
-	I/O Trans 2 Buffer Full	PC8 P7	3.0		0.0					
-	I/O Input C	PC8 P2	3.0		0.0					
-	End of Transmission	PC8 F9	3.0		0.0					
-	I/O Input A	PC8 T1	3.0		0.0					
-	I/O Input 2	PC8 G1	3.0		0.0					
-	I/O Input 1	PC8 P8	3.0		0.0					
-	I/O Input 4	PC8 L9	3.0		0.0					
-	I/O Service Request	PC8 T6	3.0		0.0					
-	I/O Trans 3 Ready to Read	PC8 J8	3.0		0.0					
-	I/O Trans 4 Hopper Empty	PC8 L8	3.0		0.0					
-	I/O Input B	PC8 D2	3.0		0.0					
-	1231 Read Gate	PC8 S9	3.0		0.0					
-	Service Response	PC8 L4					3.0		0.0	
-	I/O Disconnect	PC8 G6					3.0		0.0	
-	Select I/O Attachment	PC8 T8					3.0		0.0	
-	Process Meter	PC8 P9					3.0		0.0	
-	I/O Select	PC8 D7					3.0		0.0	
-	Reset Trans Error Latch	PC8 F4					3.0		0.0	
-	CPU Is Stopped	PC8 P3					3.0		0.0	
-	I/O Attach Read Call	PC8 M1					3.0		0.0	
-	Feed Document	PC8 T2					3.0		0.0	

30097 A

Figure 24. 1231 Optical Mark Page Reader

IBM 1403 Attachment Point (In The 1133)			Input				Output			
True Cond	Signal Name	Connector Points in 1133	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
+	Hammer 1 Fire	01C1F03A					0.0		-60.0	
+	Hammer 3 Fire	01C1F03B					0.0		-60.0	
+	Hammer 5 Fire	01C1F03C					0.0		-60.0	
+	Hammer 7 Fire	01C1F03D					0.0		-60.0	
+	Hammer 9 Fire	01C1F03E					0.0		-60.0	
+	Hammer 11 Fire	01C1F03F					0.0		-60.0	
+	Hammer 13 Fire	01C1F03G					0.0		-60.0	
+	Hammer 15 Fire	01C1F03H					0.0		-60.0	
+	Hammer 17 Fire	01C1F03J					0.0		-60.0	
+	Hammer 19 Fire	01C1F03K					0.0		-60.0	
+	Hammer 21 Fire	01C1F03L					0.0		-60.0	
+	Hammer 23 Fire	01C1F03M					0.0		-60.0	
+	Hammer 25 Fire	01C1F03N					0.0		-60.0	
+	Hammer 27 Fire	01C1F03P					0.0		-60.0	
+	Hammer 29 Fire	01C1F03Q					0.0		-60.0	
+	Hammer 31 Fire	01C1F03R					0.0		-60.0	
+	Hammer 33 Fire	01C1F04A					0.0		-60.0	
+	Hammer 35 Fire	01C1F04B					0.0		-60.0	
+	Hammer 37 Fire	01C1F04C					0.0		-60.0	
+	Hammer 39 Fire	01C1F04D					0.0		-60.0	
+	Hammer 41 Fire	01C1F04E					0.0		-60.0	
+	Hammer 43 Fire	01C1F04F					0.0		-60.0	
+	Hammer 45 Fire	01C1F04G					0.0		-60.0	
+	Hammer 47 Fire	01C1F04H					0.0		-60.0	
+	Hammer 49 Fire	01C1F04J					0.0		-60.0	
+	Hammer 51 Fire	01C1F04K					0.0		-60.0	
+	Hammer 53 Fire	01C1F04L					0.0		-60.0	
+	Hammer 55 Fire	01C1F04M					0.0		-60.0	
+	Hammer 57 Fire	01C1F04N					0.0		-60.0	
+	Hammer 59 Fire	01C1F04P					0.0		-60.0	
+	Hammer 61 Fire	01C1F04Q					0.0		-60.0	
+	Hammer 63 Fire	01C1F04R					0.0		-60.0	
+	Hammer 65 Fire	01C1F05A					0.0		-60.0	
+	Hammer 67 Fire	01C1F05B					0.0		-60.0	
+	Hammer 69 Fire	01C1F05C					0.0		-60.0	
+	Hammer 71 Fire	01C1F05D					0.0		-60.0	
+	Hammer 73 Fire	01C1F05E					0.0		-60.0	
+	Hammer 75 Fire	01C1F05F					0.0		-60.0	
+	Hammer 77 Fire	01C1F05G					0.0		-60.0	
+	Hammer 79 Fire	01C1F05H					0.0		-60.0	
+	Hammer 81 Fire	01C1F05J					0.0		-60.0	
+	Hammer 83 Fire	01C1F05K					0.0		-60.0	
+	Hammer 85 Fire	01C1F05L					0.0		-60.0	
+	Hammer 87 Fire	01C1F05M					0.0		-60.0	
+	Hammer 89 Fire	01C1F05N					0.0		-60.0	
+	Hammer 91 Fire	01C1F05P					0.0		-60.0	

Figure 25. 1403 Printer (part 1 of 5)

30098.0A

IBM 1403 Attachment Point (In The 1133)			Input				Output			
True Cond	Signal Name	Connector Points in 1133	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
+	Hammer 93 Fire	01C 1F05Q					0.0		-60.0	
+	Hammer 95 Fire	01C 1F05R					0.0		-60.0	
+	Hammer 97 Fire	01C 1F06A					0.0		-60.0	
+	Hammer 99 Fire	01C 1F06B					0.0		-60.0	
+	Hammer 101 Fire	01C 1F06C					0.0		-60.0	
+	Hammer 103 Fire	01C 1F06D					0.0		-60.0	
+	Hammer 105 Fire	01C 1F06E					0.0		-60.0	
+	Hammer 107 Fire	01C 1F06F					0.0		-60.0	
+	Hammer 109 Fire	01C 1F06G					0.0		-60.0	
+	Hammer 111 Fire	01C 1F06H					0.0		-60.0	
+	Hammer 113 Fire	01C 1F06J					0.0		-60.0	
+	Hammer 115 Fire	01C 1F06K					0.0		-60.0	
+	Hammer 117 Fire	01C 1F06L					0.0		-60.0	
+	Hammer 119 Fire	01C 1F06M					0.0		-60.0	
+	Hammer 2 Fire	01C 1E03A					0.0		-60.0	
+	Hammer 4 Fire	01C 1E03B					0.0		-60.0	
+	Hammer 6 Fire	01C 1E03C					0.0		-60.0	
+	Hammer 8 Fire	01C 1E03D					0.0		-60.0	
+	Hammer 10 Fire	01C 1E03E					0.0		-60.0	
+	Hammer 12 Fire	01C 1E03F					0.0		-60.0	
+	Hammer 14 Fire	01C 1E03G					0.0		-60.0	
+	Hammer 16 Fire	01C 1E03H					0.0		-60.0	
+	Hammer 18 Fire	01C 1E03J					0.0		-60.0	
+	Hammer 20 Fire	01C 1E03K					0.0		-60.0	
+	Hammer 22 Fire	01C 1E03L					0.0		-60.0	
+	Hammer 24 Fire	01C 1E03M					0.0		-60.0	
+	Hammer 26 Fire	01C 1E03N					0.0		-60.0	
+	Hammer 28 Fire	01C 1E03P					0.0		-60.0	
+	Hammer 30 Fire	01C 1E03Q					0.0		-60.0	
+	Hammer 32 Fire	01C 1E03R					0.0		-60.0	
+	Hammer 34 Fire	01C 1E04A					0.0		-60.0	
+	Hammer 36 Fire	01C 1E04B					0.0		-60.0	
+	Hammer 38 Fire	01C 1E04C					0.0		-60.0	
+	Hammer 40 Fire	01C 1E04D					0.0		-60.0	
+	Hammer 42 Fire	01C 1E04E					0.0		-60.0	
+	Hammer 44 Fire	01C 1E04F					0.0		-60.0	
+	Hammer 46 Fire	01C 1E04G					0.0		-60.0	
+	Hammer 48 Fire	01C 1E04H					0.0		-60.0	
+	Hammer 50 Fire	01C 1E04J					0.0		-60.0	
+	Hammer 52 Fire	01C 1E04K					0.0		-60.0	
+	Hammer 54 Fire	01C 1E04L					0.0		-60.0	
+	Hammer 56 Fire	01C 1E04M					0.0		-60.0	
+	Hammer 58 Fire	01C 1E04N					0.0		-60.0	
+	Hammer 60 Fire	01C 1E04P					0.0		-60.0	
+	Hammer 62 Fire	01C 1E04Q					0.0		-60.0	
+	Hammer 64 Fire	01C 1E04R					0.0		-60.0	
+	Hammer 66 Fire	01C 1E05A					0.0		-60.0	

30098.1A

Figure 25. 1403 Printer (part 2 of 5)

IBM 1403 Attachment Point (In The 1133)			Input				Output			
True Cond	Signal Name	Connector Points in 1133	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
+	Hammer 68 Fire	01C1E05B					0.0		-60.0	
+	Hammer 70 Fire	01C1E05C					0.0		-60.0	
+	Hammer 72 Fire	01C1E05D					0.0		-60.0	
+	Hammer 74 Fire	01C1E05E					0.0		-60.0	
+	Hammer 76 Fire	01C1E05F					0.0		-60.0	
+	Hammer 78 Fire	01C1E05G					0.0		-60.0	
+	Hammer 80 Fire	01C1E05H					0.0		-60.0	
+	Hammer 82 Fire	01C1E05J					0.0		-60.0	
+	Hammer 84 Fire	01C1E05K					0.0		-60.0	
+	Hammer 86 Fire	01C1E05L					0.0		-60.0	
+	Hammer 88 Fire	01C1E05M					0.0		-60.0	
+	Hammer 90 Fire	01C1E05N					0.0		-60.0	
+	Hammer 92 Fire	01C1E05P					0.0		-60.0	
+	Hammer 94 Fire	01C1E05Q					0.0		-60.0	
+	Hammer 96 Fire	01C1E05R					0.0		-60.0	
+	Hammer 98 Fire	01C1E06A					0.0		-60.0	
+	Hammer 100 Fire	01C1E06B					0.0		-60.0	
+	Hammer 102 Fire	01C1E06C					0.0		-60.0	
+	Hammer 104 Fire	01C1E06D					0.0		-60.0	
+	Hammer 106 Fire	01C1E06E					0.0		-60.0	
+	Hammer 108 Fire	01C1E06F					0.0		-60.0	
+	Hammer 110 Fire	01C1E06G					0.0		-60.0	
+	Hammer 112 Fire	01C1E06H					0.0		-60.0	
+	Hammer 114 Fire	01C1E06J					0.0		-60.0	
+	Hammer 116 Fire	01C1E06K					0.0		-60.0	
+	Hammer 118 Fire	01C1E06L					0.0		-60.0	
+	Hammer 120 Fire	01C1E06M					0.0		-60.0	
+	Print Latch	01C1D03E					0.0		-6.0 to -12.0	
-	Process Meter	01C1D03F					0.0		-12.0	
+	Low Speed Start Ind	01C1D02H					0.0		-6.0 to -12.0	
+	Forms Check or Carriage Stop	01C1D02P	0.0		-6.0 to -12.0					
+	Low Speed Stop Ind	01C1D02F					0.0		-6.0 to -12.0	
+	Carriage Interlock	01C1D02E	0.0		-6.0 to -12.0					
+	Print Ready Ind	01C1D03L					0.0		-6.0 to -12.0	
-	End of Forms	01C1D02M	0.0		-6.0 to -12.0					
+	Restore Key	01C1D02A	0.0		-6.0 to -12.0					
-	Restore Key	01C1D02B	0.0		-6.0 to -12.0					
-	Sense Amp	01C1D03A	0.8		-0.8					
-	Sense Amp	01C1D03B	0.8		-0.8					

30098.2A

Figure 25. 1403 Printer (part 3 of 5)

IBM 1403 Attachment Point (In The 1133)			Input				Output			
True Cond	Signal Name	Connector Points in 1133	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
+	Print Reset Key	01C1D03N	0.0		-6.0 to -12.0					
-	Magnetic Emitter	01C1D02Q	0.0		-6.0 to -12.0					
+	Magnetic Emitter Gnd	01C1D02R	0.0		-6.0 to -12.0					
-	Print Stop Key	01C1D03H	0.0		-6.0 to -12.0					
+	Print Check Ind	01C1D03D					0.0		-6.0 to -12.0	
+	Print Start Key	01C1D03G	0.0		-6.0 to -12.0					
-	Print Start Key	01C1D03J	0.0		-6.0 to -12.0					
+	Space Key	01C1D02C	0.0		-6.0 to -12.0					
-	Space Key	01C1D02D	0.0		-6.0 to -12.0					
+	End of Forms Ind	01C1D03M					0.0		-6.0 to -12.0	
+	Sync Check Ind	01C1D03C					0.0		-6.0 to -12.0	
-	UCS Emitter	01C1D02L	0.0		-6.0 to -12.0					
-	Stop Brush 1	01C1D05C	0.0		-6.0 to -12.0					
-	Stop Brush 2	01C1D05D	0.0		-6.0 to -12.0					
-	Stop Brush 3	01C1D05E	0.0		-6.0 to -12.0					
-	Stop Brush 4	01C1D05F	0.0		-6.0 to -12.0					
-	Stop Brush 5	01C1D05G	0.0		-6.0 to -12.0					
-	Stop Brush 6	01C1D05H	0.0		-6.0 to -12.0					
-	Stop Brush 7	01C1D05J	0.0		-6.0 to -12.0					
-	Stop Brush 8	01C1D05K	0.0		-6.0 to -12.0					
-	Stop Brush 9	01C1D05L	0.0		-6.0 to -12.0					
-	Stop Brush 10	01C1D05M	0.0		-6.0 to -12.0					
-	Stop Brush 11	01C1D05N	0.0		-6.0 to -12.0					
-	Stop Brush 12	01C1D05P	0.0		-6.0 to -12.0					
+	Low Speed Start*	01C1D05Q					0.0		-6.0 to -12.0	
+	Low Speed Stop*	01C1D05R					0.0		-6.0 to -12.0	
+	Forms Check Ind	01C1D05B					0.0		-6.0 to -12.0	
+	Low Speed Relay Intlk*	01C1D01M	0.0		-6.0 to -12.0					

*These lines are used to stop the carriage during power on sequence.

30098.3A

Figure 25. 1403 Printer (part 4 of 5)

IBM 1403 Attachment Point (In The 1133)			Input				Output			
True Cond	Signal Name	Connector Points in 1133	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
+	Print Conn Intlk No. 2	01C1D01J	0.0		-6.0 to -12.0					
+	Print Conn Intlk No. 1	01C1F07R					0.0		-6.0 to -12.0	
+	Chain Motor Relay Ctrl	01C1F07Q	0.0		-6.0 to -12.0					
	-6 volt DC	01C1F07G							- 6.0	
	-12 volt DC	01C1F07D							-12.0	
	-12 volt DC	01C1F07L							-12.0	
	+6 volt DC	01C1F07P					6.0			
	-6 volt DC	01C1F07H							- 6.0	
	+12 volt DC	01C1F07J					12.0			
	+12 volt DC	01C1F07K					12.0			
	-12 volt DC	01C1F07M							-12.0	
	-60 volt DC	01C1D01N							-60.0	
	Ground DC	01C1F07E					0.0			
	Ground DC	01C1F07F					0.0			

30098.4A

Figure 25. 1403 Printer (part 5 of 5)

2310 Attachment - Drive 1			Input				Output			
True Cond	Signal Name	Board	Up Level		Down Level		Up Level		Down Level	
			Volt	Ma	Volt	Ma	Volt	Ma	Volt	Ma
Gnd	CPU Clock Gate	B3B2 D10					3.0		0.0	
-	CPU Write Gate	B3B2 D11					3.0		0.0	
-	Access Go Terminated	B3B2 D04					3.0		0.0	
	DF Wr Data Terminated	B3B2 B05					3.0		0.0	
-	CPU Read Select Terminated	B3B2 B09					3.0		0.0	
+	CE Interlock	B3B2 D07					3.0		0.0	
-	CPU Head Select - Hd 1	B3B2 D09					3.0		0.0	
+	Access Direction - Forward	B3B2 B04					3.0		0.0	
-	10/20 Mil Step - 10 Mil	B3B2 B10					3.0		0.0	
-	Use Meter	B3B2 B12					3.0		0.0	
-	Access Home	B3B2 B02	3.0		0.0					
+	Access Ready	B3B2 B07	3.0		0.0					
	Raw Read Data	B3B2 D12	3.0		0.0					
-	Sector Pulses	B3B2 D06	3.0		0.0					
-	Reference Pulse	B3B2 B12	3.0		0.0					
-	Drive Ready	B3B2 D13	3.0		0.0					
-	Write Select Error	B3B2 B08	3.0		0.0					
	90 Sec Time Delay	B3B2 D02	3.0		0.0					

30099A

Figure 26. 2310 Model B, Drive 1

When a transmission line is supplied by a single driver and feeds a single receiver, the driver and receiver must be located at the extreme ends of the lines. A driver or receiver can be located beyond the line terminator, provided that the line length between the driver or receiver is less than six inches.

Power and Signal Cabling

The power and signal cable connector locations within the 1131 and 1133 are shown in the following figures:

1130 system external cables: Figure 27.
Power and signal connector panel (1131): Figure 28.
1442 power connections: Figure 29.
1132 power connections: Figure 30.
2501 power connections: Figure 31.
SAC sequence power connections: Figure 32.
I/O signal panel (1131): Figure 33.
1627 signal connections: Figure 34.
1131 console printer signal connections: Figure 35.
1055 signal connections: Figure 36.
1134 signal connections: Figure 37.
SMS power panel (PP) I/O device connections: Figures 38 and 39.
Single Disk Storage dc voltage connections: Figure 40.
I/O cable connector interface panel CC (1133): Figure 41.
SAC II power sequence connections: Figure 42.
1403 power connections: Figure 43.
2310 ac power connections: Figure 44.
2310 dc power connections: Figure 45.

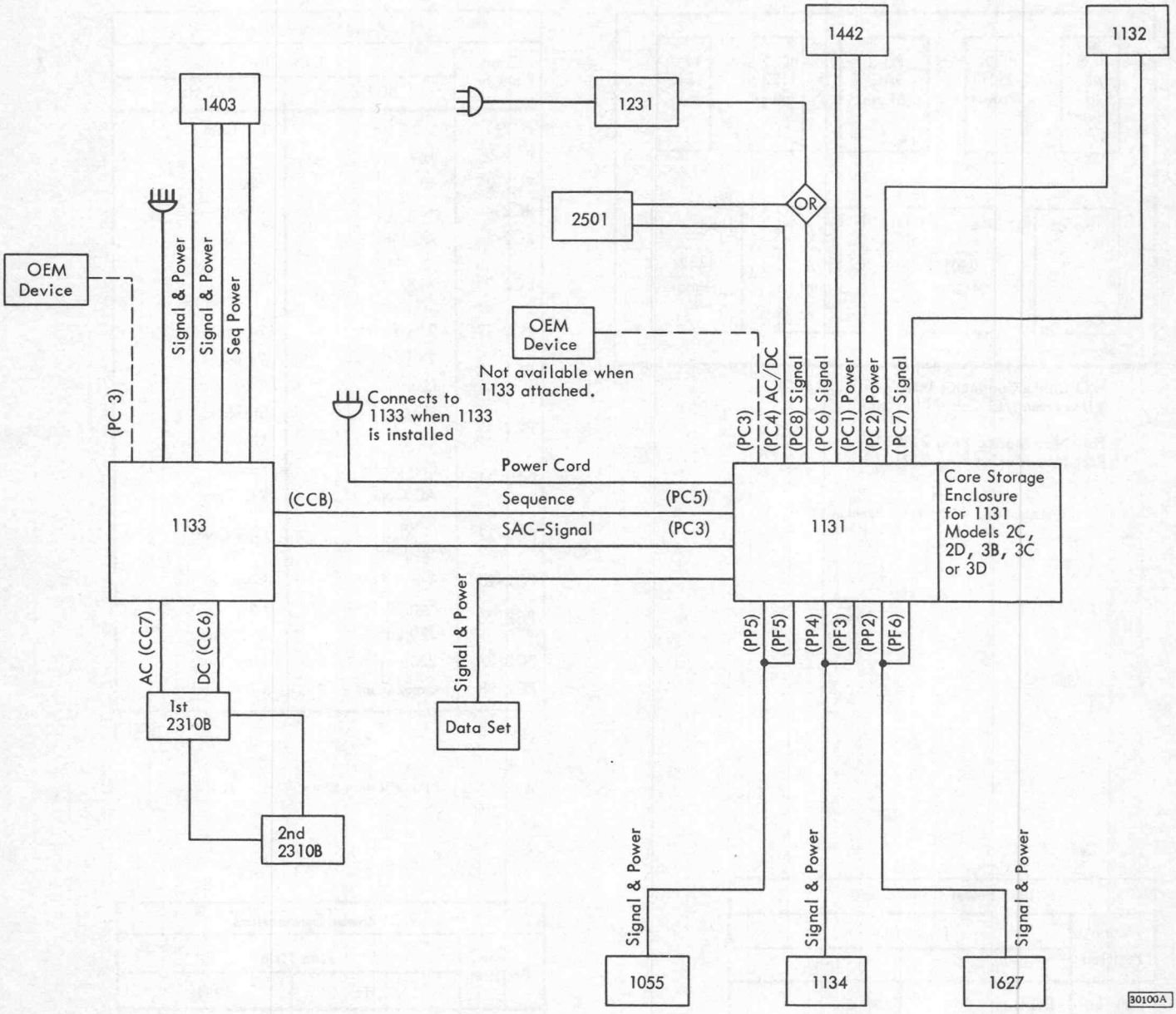
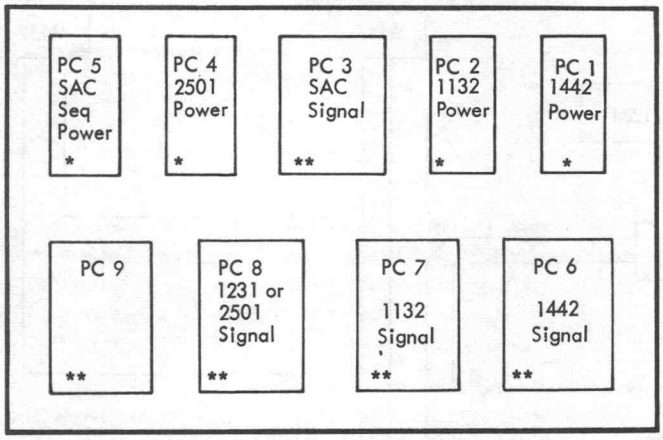


Figure 27. 1130 System External Cable Connections



I/O Cable Connector Interface Panel (PC)
View From I/O Cable Plug Side

* Part No. Mating Plug 2180672
** Part No. Mating Plug 2191078

11413C

Figure 28. Power and Signal Connector Panel in 1131

1132 Power Connections		
Conn Position	Line Title	
	50 Hz	60 Hz
PC2-1	DC Com	DC Com
PC2-2	+6v	+6v
PC2-3	+3v	+3v
PC2-4	-3v	-3v
PC2-6	AC Gnd	AC Gnd
PC2-9	+12v	+12v
PC2-17	24 vac	24 vac
PC2-18	24 vac Com	24 vac Com
PC2-19	Shield Gnd	Shield Gnd
PC2-21	Fan AC Com	Fan AC Com
PC2-22	220v AC Com	Line Com
PC2-23	Conv ac	Conv ac
PC2-26	Fan 220 vac	Fan 115 vac
PC2-27	220 vac	Line V
PC2-28	Conv Com	Conv Com

30102

Figure 30. 1132 Power Connections

1442 Power Connections		
Conn Position	Line Title	
	50 Hz	60 Hz
PC1-1	DC Com	DC Com
PC1-2	+6v	+6v
PC1-3	+3v	+3v
PC1-4	-3v	-3v
PC1-6	AC Gnd	AC Gnd
PC1-9	Spare	Spare
PC1-17	SCR ac	SCR ac
PC1-18	SCR Com	SCR Com
PC1-19	Shield Gnd	Shield Gnd
PC1-21	Fan AC Com	Fan AC Com
PC1-22	220 vac AC Com	Line Com
PC1-23	Conv ac	Conv ac
PC1-26	Fan 220 vac	Fan 115 vac
PC1-27	220 vac	Line V
PC1-28	Conv Com	Conv Com

30101

Figure 29. 1442 Power Connections

2501 Power Connections		
Conn. Position	Line Title	
	50 Hz	60 Hz
PC4-2	+6	+6
PC4-1	Gnd	Gnd
PC4-3	+3	+3
PC4-4	-3	-3
PC4-22	208 Com	208 Com
PC4-27	208 ac	208 ac
PC4-28	115 Com	115 Com
PC4-23	115 ac	115 ac
PC4-6	AC Gnd	AC Gnd
PC4-18	7.25 Com	7.25 Com
PC4-17	7.25 ac	7.25 ac
PC4-19	Shield	Shield

30103

Figure 31. 2501 Power Connections

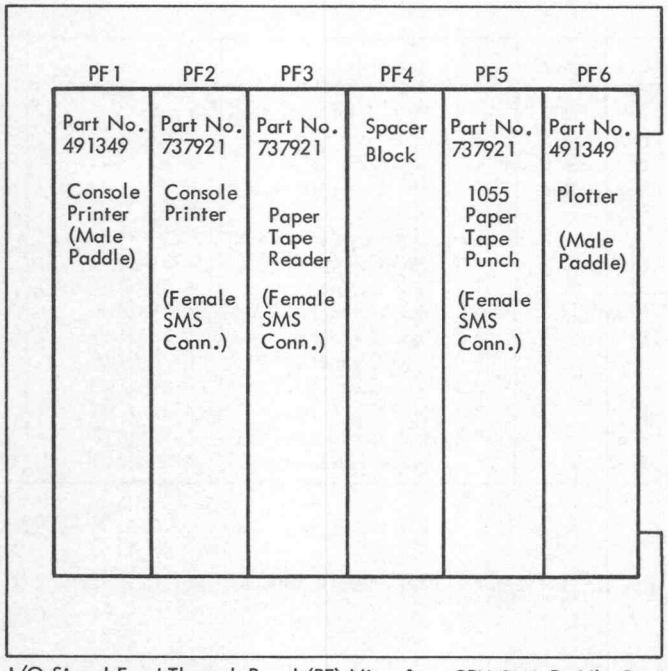
SAC Power Sequence			
1131 to SAC I or 1133		1133 to SAC II	
Line Title	Connector Position	Line Title	Connector Position
Convenience AC	PC5-17		
Convenience Common	PC5-18		
SAC Shield Ground	PC5-19		
Emergency Power Off Switch	PC5-21	SAC II Emergency Power Off Switch	CC5-23**
Emergency Power Off Switch	PC5-26	SAC II Emergency Power Off Switch	CC5-28**
SAC Sequence 24 Vac	PC5-22	SAC II Sequence 24 Vac	CC5-22
SAC Sequence 24 Vac Com.	PC5-27	SAC II Sequence 24 Vac Com.	CC5-27
SAC Emergency Power Off	PC5-23*	SAC II Emergency Power Off	CC5-21
SAC Emergency Power Off	PC5-28*	SAC II Emergency Power Off	CC5-26

* If SAC device is not using PC5, then jumper PC5-23 to PC5-28.

** If SAC II device is not using CC5, then jumper CC5-23 to CC5-28.

30104A

Figure 32. SAC Sequence Power Connections



I/O Signal Feed Through Panel (PF) View from CPU-SMS Paddle Card Side.

11415A

Figure 33. I/O Signal Panel

Connection	Line Title	Connection	Plug P5
-	PF6A to 6F No Connection	-	-
A-C1N5B10	-24v Ready	PF6G	16
-	--	PF6H	N.C.
-	No Connection	PF6J	-
-	No Connection	PF6K	-
A-C1N5D05	-Pen Down Drive	PF6L	12
A-C1N5B04	-Pen Up Drive	PF6M	11
A-C1N5D04	-Carr Left Drive	PF6N	7
A-C1N5B03	-Carr Right Drive	PF6P	8
A-C1N5D02	-Drum Down Drive	PF6Q	6
A-C1N5B02	-Drum Up Drive	PF6R	5

11417

Figure 34. 1627 Plotter Signal Connections

Connection	Line Title	Connection
A-C1A4B02	-Select T2	PF1A
A-C1A4D02	-Select T1	PF1B
A-C1A4B03	-Select R2A	PF1C
A-C1A4D04	-Select R1	PF1D
A-C1A4B04	-Select R5	PF1E
A-C1A4D05	-Select R2	PF1F
A-C1A4B05	-Select Aux	PF1G
A-C1A4D06	-Line Feed	PF1H
A-C1A4B07	-Tab	PF1J
A-C1A4D07	-Cr-Lf and EOL	PF1K
A-C1A4B08	-Up Shift	PF1L
-	No Connection	PF1M
-	No Connection	PF1N
-	No Connection	PF1P
-	No Connection	PF1Q
A-C1A4D09	-Down Shift	PF1R
PF2A	+Twr End Of Line	A-C1A4B09
PF2B	No Connection	-
PF2C	+12v E.O.L. Input	PF2L
PF2D	No Connection	-
PF2E	-Twr CB Response	A-C1A4D10
PF2F	Car Ret Inlk	Not Used
PF2G	Crlft Inlk 2	Not Used
A-C1A4B10	-Space	PF2H
A-C1A4D11	-Backspace	PF2J
A-C1A4B12	-Black Ribbon Shift	PF2K
PF2L	-Twr End Of Forms	A-C1A4D12
PF2M	No Connection	-
PF2N	+Twr Crlft Inlk	A-C1A4B13
A-C1A4D13	-Red Ribbon Shift	PF2P
Not Used	Double Line Feed	PF2Q
Not Used	Single Line Feed	PF2R

11416

Figure 35. 1131 Console Printer Connections

Connection	Line Title	Connection
PF5A	Backspace Punch	Not Used
-	R & S Counter	PF5B
PF5C	No Connection	-
PF5D	No Connection	-
PF5E	No Connection	-
A-B1N5D04	-Drive P.T. Punch Clutch	PF5F
A-B1N5B08	-P.T. Punch 8th Chan Drive	PF5G
PF5H	-P.T. Punch Ready	A-B1N5B03
PF5J	GND 8th Chan	Not Used
A-B1N5B09	-P.T. Punch C Drive	PF5K
A-B1N5D06	-P.T. Punch 1 Drive	PF5L
A-B1N5B10	-P.T. Punch 2 Drive	PF5M
A-B1N5D10	-P.T. Punch 4 Drive	PF5N
A-B1N5B13	-P.T. Punch 8 Drive	PF5P
A-B1N5D07	-P.T. Punch A Drive	PF5Q
A-B1N5B07	-P.T. Punch B Drive	PF5R

11418

Figure 36. 1055 Paper Tape Punch Signal Connections

Connection	Line Title	Connection
A-B1A6D02	-P.T. Rdr. Clutch Drive B	PF3A
Not Used	Reverse Drive A	PF3D
Not Used	Reverse Drive B	PF3E
A-B1A6D06	-P.T. Rdr. Clutch Drive A	PF3F
-	No Connection	PF3G
-	No Connection	PF3H
PF3K	-P.T. Read Contact C	A-B1A6B10
PF3L	-P.T. Read Contact 1	A-B1A6B04
PF3M	-P.T. Read Contact 2	A-B1A6B05
PF3N	-P.T. Read Contact 4	A-B1A6D07
PF3P	-P.T. Read Contact 8	A-B1A6D09
PF3Q	-P.T. Read Contact A	A-B1A6D13
PF3R	-P.T. Read Contact B	A-B1A6D12
PF3C	-P.T. Read Contact 8th CH	A-B1A6B12
PF3B	-P.T. Reader Ready	A-B1A6B03

11419A

Figure 37. 1134 Paper Tape Reader Signal Connections

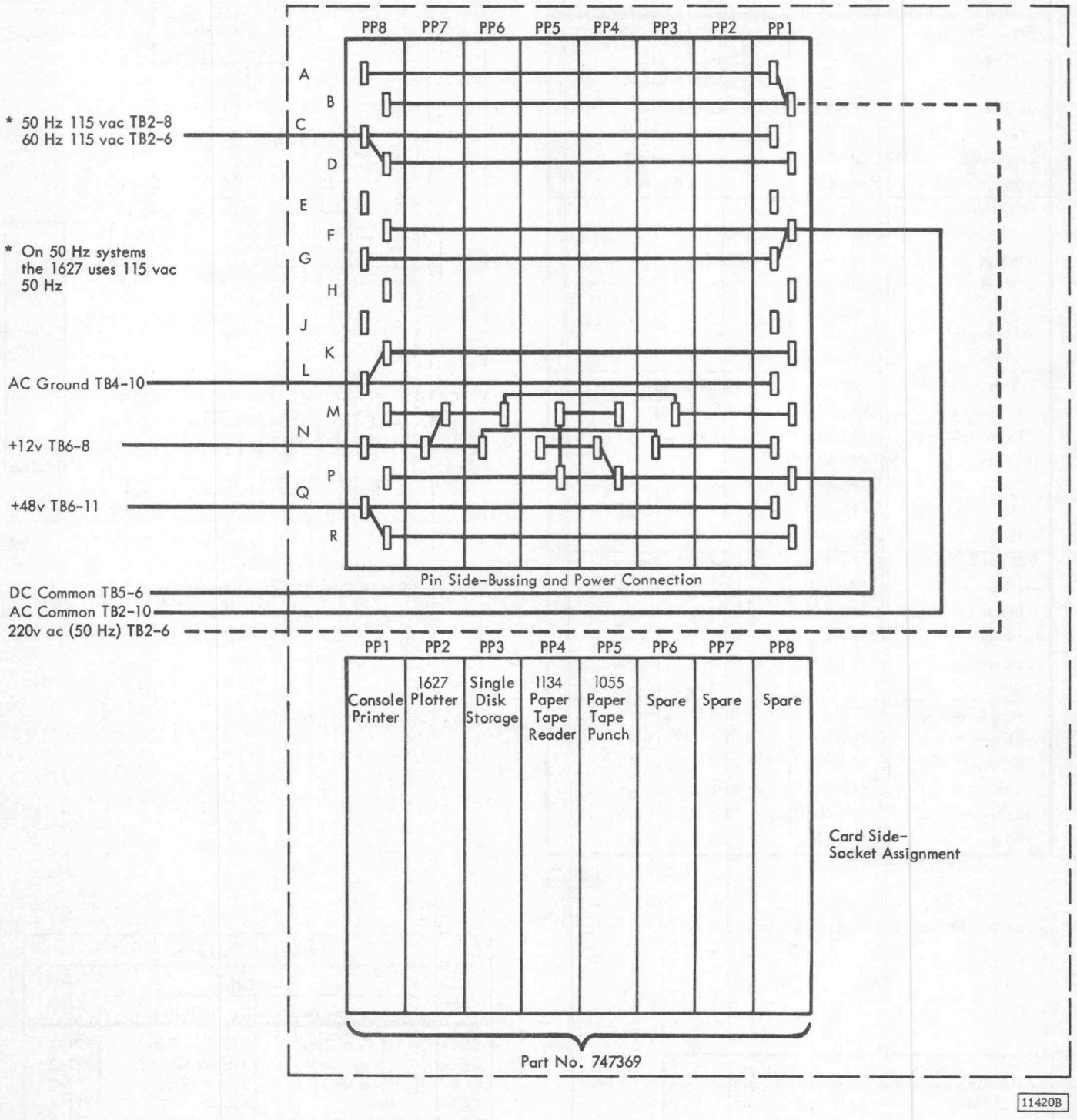


Figure 38. SMS Power Panel (PP)

Voltage	Connector Position	I/O Device
220 vac (50 Hz)	PP1-AB	
ac Common	PP1-FG	Console Printer
115 vac (60 Hz)	PP1-CD	Console Printer
ac Gnd	PP1-KL	Console Printer
+12v	PP1-MN	Console Printer
dc Common	PP1-P	Console Printer
+48v	PP1-QR	Console Printer
Not Used	PP2-AB	
ac Common	PP2-FG	Plotter
115 vac	PP2-CD	Plotter
ac Gnd	PP2-KL	Plotter
+12v	PP2-MN	
dc Common	PP2-P	Plotter
+48v	PP2-QR	
220 vac (50 Hz)	PP3-AB	Disk Storage
ac Common	PP3-FG	Disk Storage
115 vac (60 Hz)	PP3-CD	Disk Storage
ac Gnd	PP3-KL	-
+12v	PP3-MN	-
dc Common	PP3-P	-
+48v	PP3-QR	-
220 vac (50 Hz)	PP4-AB	1134 P. T. Reader
ac Common	PP4-FG	1134 P. T. Reader
115 vac (60 Hz)	PP4-CD	1134 P. T. Reader
ac Gnd	PP4-KL	1134 P. T. Reader
dc Common	PP4-MNP	1134 P. T. Reader
+48v	PP4-QR	1134 P. T. Reader
220 vac (50 Hz)	PP5-AB	1055 P. T. Punch
ac Common	PP5-FG	1055 P. T. Punch
115 vac (60 Hz)	PP5-CD	1055 P. T. Punch
ac Gnd	PP5-KL	1055 P. T. Punch
dc Common	PP5-MNP	1055 P. T. Punch
+48v	PP5-QR	1055 P. T. Punch

11421B

Figure 39. SMS Power Panel (PP) I/O Device Connections

1131 Connection	Voltage
TB5-2	dc Common
TB5-10	-3vdc
TB6-1	+6vdc
TB6-4	+3vdc
TB6-11	+48vdc

11422

Figure 40. Single Disk Storage DC Voltage Connections

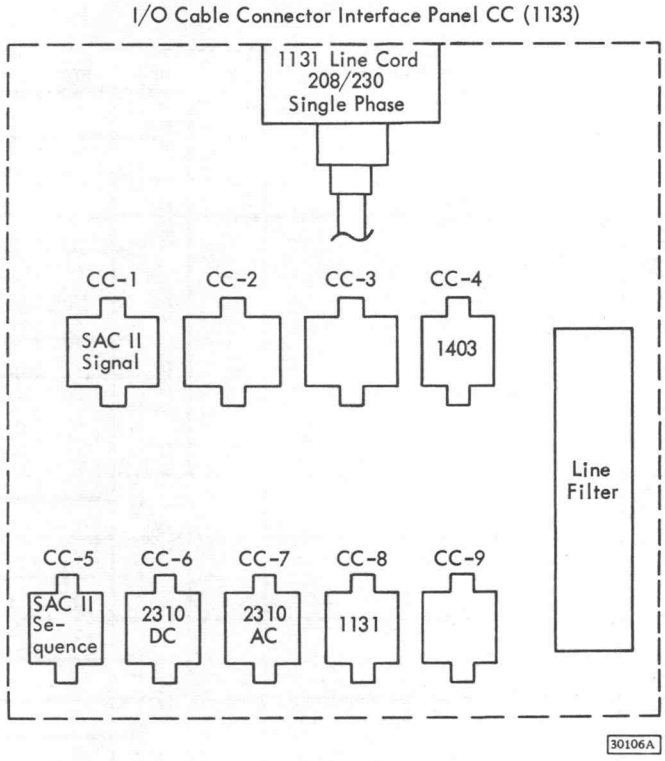


Figure 41. I/O Cable Connector Interface Panel CC (1133)

1403 Power Connector			
1133 Conn	Line Title		1403 Conn
	50 Hz	60 Hz	
CC4-1	115 Com Conv	115 Com Conv	PP1-1
CC4-2	115 vac Conv	115 vac Conv	PP1-2
CC4-3	Frame Gnd	Frame Gnd	PP1-3
CC4-4	-60vdc	-60vdc	PP1-4
CC4-8	Chain + RBN Motor	Chain + RBN Motor	PP1-8
CC4-9	Chain + RBN Motor	Chain + RBN Motor	PP1-9
CC4-11	Ph 1 Carr Motor	Ph 1 Carr Motor	PP1-11
CC4-12	Ph 2 Carr Motor	Ph 2 Carr Motor	PP1-12
CC4-13	Ph 3 Carr Motor	Ph 3 Carr Motor	PP1-13

30108

Figure 42. 1403 Power Connections

2310B AC Power Connector		
1133 Conn	Line Title	
	50 Hz	60 Hz
CC7-1	Phase 1	Phase 1
CC7-2	115 Com Conv	115 Com Conv
CC7-3	Phase 3	Phase 3
CC7-4	115 vac Conv	115 vac Conv
CC7-13	Phase 2	Phase 2
CC7-14	Neutral	Not Used
CC7-19	Frame Gnd	Frame Gnd
CC7-24	24 Com Seq Cont	24 Com Seq Cont
CC7-25	24 vac Seq Cont	24 vac Seq Cont

30109

Figure 43. 2310 Model B AC Power Connections

2310B DC Power Connector		
1133 Conn	Line Title	
	50 Hz	60 Hz
CC6-1	+6vdc Logic	+6vdc Logic
CC6-3	DC Com	DC Com
CC6-4	DC Com	DC Com
CC6-10	DC Com	DC Com
CC6-13	+3vdc Logic	+3vdc Logic
CC6-19	-3vdc Logic	-3vdc Logic

30110

Figure 44. 2310 Model B DC Power Connections

APPENDIX. GLOSSARY

Most of the definitions within this glossary are standard to the data processing industry; however, some definitions are unique to this publication.

Adapter: In general, the logic necessary to control a particular I/O device and adapt its signals to a common mode.

Accumulator: The register which holds the resultant data following an arithmetic or logical operation.

Address: Location; in 1130 main storage each word (group of 16 bits) is addressable. Also, the location of records in other storage media, such as disk.

Address Register: A register that stores an address.

Asynchronous: Indicates that the execution of one operation is dependent on a signal that a prior operation is completed.

Auxiliary Storage: Any on-line storage media other than CPU main storage.

Binary: The base-2 numbering system.

Binary-Coded-Decimal: A means of designating a string of binary digits for easier comprehension (units position equals 1, the next higher position equals 2; the next higher equals 4, etc.)

Bit: A binary digit (either 0 or 1; generally the 1 is considered a bit and the 0 is a no-bit).

Central Processing Unit (CPU): The unit of a processing system that contains the logical circuits which control the execution of instructions and the access to main storage of the system.

Channel: A path along which signals can be sent. Also, a unit that controls the operation of one or more I/O units.

Clock: A device that generates periodic signals used for synchronization.

Code: The assignment of meaning to a character relative position.

Command: In general, within the 1130 system, a command performs a function associated with an I/O device and, therefore, must use an Input/Output Control Command.

Communication: The process of transferring information from one place to another.

Core Storage: Storage media using magnetic cores; generally, main storage.

Cycle: An interval of time in which one set of events is completed.

Cycle-Steal Operation: A means of increasing useful CPU time by allowing each I/O device to take only the CPU time necessary to transfer a data character. Generally, one CPU cycle for each character transferred. See also synchronous.

Data: Any representation of characters, signals, etc., to which meaning can be assigned.

Decimal: The base-10 numbering system.

Execute: To carry out an instruction or command.

Execution Cycle: That portion (or time) of the CPU function that is necessary to perform the resultant command determined by a prior instruction cycle(s).

Function: For the 1130, specifies one of seven input or output operations to be performed.

Hexadecimal: A numbering system using the equivalent of the decimal number 16 as a base.

Index Register: A register whose contents is added to or subtracted from the operand address prior to or during the execution of an instruction.

Indirect Address: A word in main storage that is used by the CPU as an address but is located, indirectly, by using the contents of the address specified by the program, rather than the specified address itself.

Input: The data that is received by the CPU for processing and/or manipulation. Input data may be in a variety of forms: punched cards or tape, magnetic disk or tape, telephone communication, manual keyboard, etc.

I/O: Input/Output

Input/Output Control Command (IOCC): Two consecutive words in 1131 main storage that contain the address, area or device code, function, and modifier bits, for input or output operations. The first word of the IOCC must be at an even address.

Instruction: In general, within the 1130 system, an instruction performs a CPU function not associated with an I/O device, such as add, subtract, or branch. The one exception is the XIO instruction which interrogates an IOCC that, in turn, becomes an I/O command.

Instruction Address Register: The register that holds the storage address of the next instruction in sequence following the instruction currently being performed.

Instruction cycle: That portion (or time) of the CPU function that is necessary to decode the instruction code to determine the function to be performed.

Interface: The shared boundary connecting logic between devices.

Interrupt Operation: A means of increasing useful CPU time by allowing more than one function to be performed at a time. Each I/O device literally interrupts the CPU for only the time necessary to service it. See also asynchronous.

Load: To place data into a storage media, such as core storage.

Logic: The basic principle which governs applications, switching, gating, electronics, etc.

Machine Instruction: An instruction recognized and executed by a particular machine.

Modifier: A means of expanding or modifying a basic instruction to allow one instruction to perform a variety of related functions.

Multiplex Operation: The interleaving or simultaneous transfer of more than one group of signals along a common data path.

Off-Line: Pertaining to peripheral equipment or devices not in direct communication with the CPU.

On-Line: Pertaining to peripheral equipment or devices in direct communication with the CPU.

Operation code: The logical code recognized by the CPU to initiate an operation or function.

Output: The data that is produced by the CPU, generally after a logical function has been performed on it. Output data may be in many forms: printed forms, punched cards or tape, magnetic disk or tape, etc.

Signal Lines: The physical wires that carry signals between two or more devices.

Storage Address Register: The register that holds the storage address during the execution of an instruction.

Storage Cycle: The time interval required to access (either input or output) a word in main storage.

Synchronous: In synchronization.

Transmission Lines: Signal lines.

Two's Complement: A means of storing binary digits in a storage media so as to reflect the quantity as negative; it is accomplished by inverting the binary digits (a zero becomes a one; a one becomes a zero) and then logically adding one to the units position.

Word: A group of consecutive bits. In the 1131 CPU main storage, a word is 16 bits, and is the smallest addressable unit.

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